Service Manual

Chassis

11 AK 52 B

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1.INTRODUCTION

11AK52 is a 100Hz flicker free colour television capable of driving 28"4:3/16:9, 32" 16:9, 33"4:3 and 29"4:3 real flat picture tubes.
The chassis is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L´.
Sound system output is supplying 2x10W (10%THD) for left and right outputs of 8ohm speakers.
TV supports the level 1.5 teletext standard. It is possible to decode transmissions including high graphical data.
The chassis is equipped with two full EuroScarts, one SCART for AV input/output, one front-AV input, one back-AV input, one headphone output, one SVHS input (via SCART and SVHS connector), two external speaker outputs (left and right).

2.TUNER

The hardware and software of the TV is suitable for tuners, supplied by different companies, which are selected from the Service Menu. These tuners can be combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L´, I/I´, and D/K. The tuning is available through the digitally controlled I^2C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

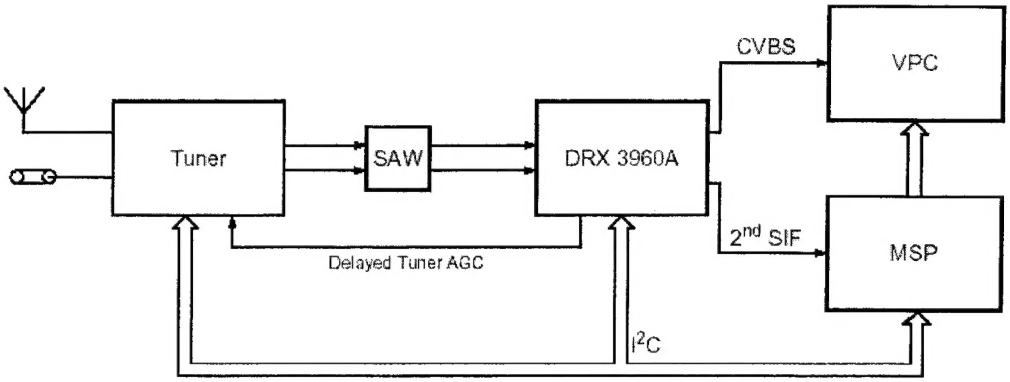
Features of UV1316:
1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
3. Digitally controlled (PLL) tuning via I^2C-bus
4. Off-air channels, S-cable channels and Hyperband
5. World standardized mechanical dimensions and world standard pinning
6. Compact size
7. Complies to "CENELEC EN55020" and "EN55013"

Pinning:

1.	Gain control voltage (AGC)	:	4.0V, Max: 4.5V
2.	Tuning voltage		
3.	I^2C-bus address select	:	Max: 5.5V
4.	I^2C-bus serial clock	:	Min:-0.3V, Max: 5.5V
5.	I^2C-bus serial data	:	Min:-0.3V, Max: 5.5V
6.	Not connected		
7.	PLL supply voltage	:	5.0V, Min: 4.75V, Max: 5.5V
8.	ADC input		
9.	Tuner supply voltage	:	33V, Min: 30V, Max: 35V
10.	Symmetrical IF output 1		
11.	Symmetrical IF output 2		

3.IF PART (DRX 3960A)

Tuner output IF signal is pre-filtered with only one 8-MHz channel SAW filter. The entire multistandard processing is performed. The Digital Receiver Front-end DRX 3960A performs the entire multi-standard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF). Video and tuner AGC is controlled and adjusted by take over voltage. The alignment-free DRX 3960A needs no special external components. All control functions and status registers are accessible via I^2C bus interface.



4.VIDEO SWITCH TEA6415

In case of three or more external sources are used, the video switch IC TEA6415 is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS. Driving 75ohm load needs an external resistor. It is possible to have the same input connected to several outputs.

5.MULTI STANDARD SOUND PROCESSOR

The MSP34x1G family of single-chip Multi-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Signal conforming to the standard by the Broadcast Television Systems Committee (BTSC).
The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

6.SOUND OUTPUT STAGE WITH TDA7480L

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially designed for high efficiency applications mainly for TV and Home Stereo sets.
Mute stand-by function of the audio amplifier can be described as the following; the pin 12 (MUTE/STAND-BY) controls the amplifier status by two different thresholds, referred to ground. When Vpin 12 voltage is lower than 0.7V the amplifier is in Stand-by mode and the final stage generators are off. When Vpin 12 is higher than 4V, the amplifier is in play mode.
The TDA7480L is a 10W+10W stereo sound amplifier with mute/stand-by facility. MUTE control signal coming from microcontroller (when it is at high level) activates the mute function. IC is muted when mute pin is at low level (pin12). MUTE pin can also be activated via an external pop-noise circuitry in order to eliminate pop noise when TV is turned off. Just after the TV is turned off, this circuit switches the IC to stand-by mode by pulling the mute pin voltage to ground.

7.VERTICAL OUTPUT STAGE WITH TDA8177F

The IC TDA8177F is the vertical deflection booster circuit. Two supply voltages, +12V and -12V are needed to scan the inputs VERT+ and VERT-, respectively. And a third supply voltage, +60V for the flyback limiting are needed. The vertical deflection coil is connected in series between the output and feedback to the input.

8.VIDEO OUTPUT AMPLIFIER TDA6109

The TDA6109 includes three video output amplifiers in order to drive the three cathodes of a colour picture tube directly. To obtain maximum performance, the amplifier is used with black-current control.

9.POWER SUPPLY (SMPS)

The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer generates 135V for FBT input, +/-14V for audio amplifier, 8V stand by voltage and 8V, 12V and 5V supplies for other different parts of the chassis.

An optocoupler is used to control the regulation of line voltage and stand-by power consumption. There is a regulation circuit in secondary side. This circuit produces a control voltage according to the changes in 135V DC voltage, via an optocoupler (TCET 1102G) to pin3 of the IC.

During the switch on period of the transistor, energy is stored in the transformer. During the switch off period energy is fed to the load via secondary winding. By varying switch-on time of the power transistor, it controls each portion of energy transferred to the second side such that the output voltage remains nearly independent of load variations.

10.MICROCONTROLLER SDA5550

10.1.General Features

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V
- ROM version is used.

10.2.External Crystal and Programmable Clock Speed

- Single external 6MHz crystal, all necessary clocks are generated internally
- CPU clock speed selectable via special function registers.
- Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

10.3.Microcontroller Features

- 8bit 8051 instruction set compatible CPU.
- 33.33-MHz internal clock (max.)
- 0.360 ms (min.) instruction cycle
- Two 16-bit timers
- Watchdog timer
- Capture compare timer for infrared remote control decoding
- Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
- ADC (4 channels, 8 bit)
- UART (rxd, txd)

10.4.Memory

- Up to 128 Kilobyte on Chip Program ROM
- Eight 16-bit data pointer registers (DPTR)
- 256-bytes on-chip Processor Internal RAM (IRAM)
- 128bytes extended stack memory.
- Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
- UP to 16KByte on Chip Extended RAM (XRAM) consisting of;

- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

10.5.Display Features

- ROM Character set supports all East and West European Languages in single device
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters
- Variable Flash Rate
- Programmable Screen Size (25 Rows x 33...64 Columns)
- Flexible Character Matrixes (HxV) 12 x 9...16
- Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
- CLUT with up to 4096 colour combinations
- Up to 16 Colours per DRCS Character
- One out of 8 Colours for Foreground and Background Colours for 1-bit DRCS and ROM Characters

10.6.ROM Characters

- Shadowing
- Contrast Reduction
- Pixel by Pixel Shiftable Cursor With up to 4 Different Colours
- Support of Progressive Scan and 100 Hz.

• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

10.7.Acquisition Features

• Multi-standard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

10.8.Ports

• One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port0)
• Two 8-bit multifunction I/O-ports (Port1, Port3)
• One 4-bit port working as digital or analogue inputs for the ADC (Port2)
• One 2-bit I/O port with secondary function (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

11.SERIAL ACCESS 32K EEPROM

24LC32 is the 32Kbit electrically erasable programmable memory. The memory is compatible with the I^2C standard, two wire serial interface, which uses a bi-directional data bus and serial clock.

12.CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

13.SAW FILTERS

X6966M is an 8-MHz SAW Filter which is used for pre-filtering the IF input signal of DRX 3960A. The entire multistandard processing is performed within this filter which limits the signal bandwidth to 8 MHz and suppresses major parts of the adjacent channels.

14.IC DESCRIPTIONS

TDA6109
27W401
24LC32
SDA5275
DRAM 4MX4
SDA9400
LM317T
DDP3310
SDA5550
TEA6415
VPC3230D
TDA1308T
MSP3411G
TL431
DRX3960A
LM7808
BDX53BFI
TDA8177F
LM1086
MC44608
TCET1102G
TDA7480L
SAA3010T

14.1.TDA6109

14.1.1.General Description

The TDA6109JF includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control.

14.1.2.Features

· Typical bandwidth of 9.0 MHz for an output signal of 60 V (p-p)
· High slew rate of 1850 V/ms
· No external components required
· Very simple application
· Single supply voltage of 200 V
· Internal reference voltage of 2.5 V
· Fixed gain of 51
· Black-Current Stabilization (BCS) circuit
· Thermal protection.

14.1.3.Pinning

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

14.2.27W401

14.2.1.Description

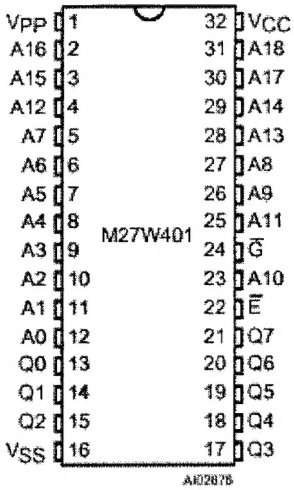
The M27W401 is a low voltage 4 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organized as 524,288 by 8 bits. The M27W401 operates in the read mode with a supply voltage as low as 2.7V at –40 to 8? ? C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery re-charges.
The FDIP32W (window ceramic frit-seal package) has a transparent lid, which allows the user to ex-pose the chip to ultraviolet light to erase the bit pat-tern. A new pattern can then be written to the device by following the programming procedure. For application where the content is programmed only one time and erasure is not required, the M27W401 is offered in PDIP32, PLCC32 and TSOP32 (8 x 20 mm) packages.

14.2.2.Features

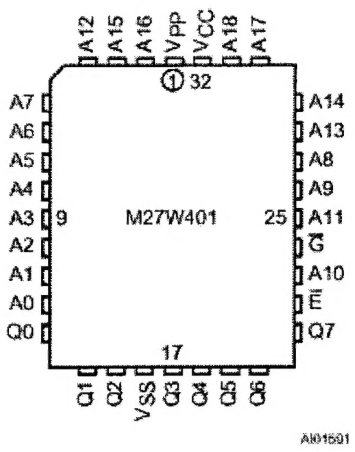
2.7V to 3.6v Low voltage in Read Operation
Access time:
–70ns at V_{CC} = 3.0V to 3.6V
–80ns at V_{CC} = 2.7V to 3.6V
Pin Compatible with M27C4001
Low Power Consumption:
–1? mA max Standby Current
– 15mA max Active Current at 5MHz
Programming Time 10?s/byte
High Reliability CMOS Technology
– 2,000V ESD Protection
– 200mA Latchup Protection Immunity

Electronic Signature
– Manufacturer Code: 20h
– Device Code: 41h

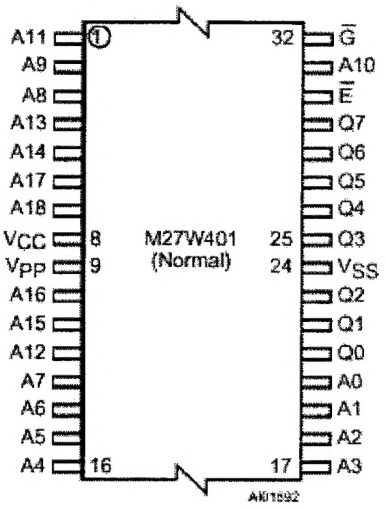
14.2.3.Connections



DIP connections



LCC Connections



TSOP Connections

Signal Names

A0-A18	Address Inputs
Q0-Q7	Data Outputs
E	Chip Enable
G	Output Enable
V_{pp}	Program Supply
V_{cc}	Supply Voltage
V_{ss}	Ground

14.3.24LC32A

14.3.1.Description

The Microchip Technology Inc. 24LC32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32A also has a page-write capability of up to 32 bytes of data. The 24LC32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24LC32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/ low-voltage, nonvolatile code and data applications. The 24LC32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packaging.

14.3.2.Features

- Single supply with operation down to 2.5V
- Maximum write current 3 mA at 6.0V
- Standby current 1 mA max at 2.5V
- 2-wire serial interface bus, I 2 CÔ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32 byte page or byte write modes available

• Schmitt trigger filtered inputs for noise suppression
• Output slope control to eliminate ground bounce
• 2 ms typical write cycle time, byte or page
• Up to eight devices may be connected to the same bus for up to 256K bits total memory
• Electrostatic discharge protection > 4000V
• Data retention > 200 years
• 8-pin PDIP and SOIC packages
• Temperature ranges
• Commercial (C): 0°C to +75°C
• Industrial (I): -40°C to +85°C

14.3.3.Pin Descriptions

A0, A1, A2 Chip Address Inputs
The A0..A2 inputs are used by the 24LC32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte.

SDA Serial Address/Data Input/Output
This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull up resistor to Vcc (typical 10 kO for 100 kHz, 2 kO for 400 kHz) For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock
This input is used to synchronize the data transfer from and to the device.
WP
This pin must be connected to either Vss or Vcc. If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-FFF). If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.
Wcc
+2.5V to 6V Power Supply
Wss
Ground

14.4.SDA5275

14.4.1.Features

• Single chip teletext IC
• Analog CVBS-input with onchip clamping circuitry
• Slicer
• Supports level 1, 2.5 and 3.5 ETSI teletext standard
• Stores up to 14 teletext pages on chip
• Stores up to 2048 teletext pages with external 16 M memory
• SDA 5275: full level 2.5 processing
• Analog RGB-output
• 41 Latin script languages
• 12 ´ 10 character size
• Parallel display attributes
• 64 from 4096 colors selectable
• Enhanced flash modes
• Dynamically redefinable character set (DRCS, PCS)
• Pixel graphics
• Full screen display (64 ´ 32 or 80 ´ 24 character positions)
• Horizontal and vertical scrolling
• Graphic cursors
• 4:3 and 16:9 display
• Multinorm display (50/60/100/120 Hz)
• RISC-processor
• Firmware downloadable
• I^2C / 3 wire UART-interface (1 Mbit/s)
• Independent clocks for acquisition and display

• Tools for greatly simplified software development
• 24-Kbyte on-chip reconfigurable DRAM
• 44160-bit character ROM
• One external crystal for all standards

14.4.2.Pin Definition and functions

Pin No. P-LCC-68-1	Symbol	Function
1	INTQ	Interrupt request output to ext. controller
2	CLK-IO	System clock input/output
3	TCSQ/FLD	Composite sync output/ field output
4	VS/VCS	Vertical sync input/output
5	HS	Horizontal sync input/output
6	XOUT	20.5-MHz crystal oscillator output
7	XIN	20.5-MHz crystal oscillator input
8	GPO	General purpose output
9	TM	Test pin, leave open or connect VSS
10	CVBS	CVBS-video signal input
11	VDD1	+ 5 V digital supply
12	VDDA	+ 5 V analog supply
13	VSSA1	Analog ground
14	N.C.	Not connected
15	N.C.	Not connected
16	VDD2	+ 5 V digital supply
17	RES	Chip reset
18	N.C.	Not connected
19	N.C.	Not connected
20	N.C.	Not connected
21	VDD3	+ 5 V digital supply
22	N.C.	Not connected
23	VREF	+ 3 V reference voltage input
24	N.C.	Not connected
25	VDD4	+ 5 V digital supply
26	A8	External DRAM-address
27	A7	External DRAM-address
28	A6	External DRAM-address
29	A5	External DRAM-address
30	A4	External DRAM-address
31	A3	External DRAM-address
32	A2	External DRAM-address
33	A1	External DRAM-address
34	A0	External DRAM-address
35	A9	External DRAM-address
36	A10	External DRAM-address
37	A11	External DRAM-address
38	RASQ	Row address strobe (DRAM)
39	WEQ	Write enable (DRAM)
40	D1	External DRAM-data
41	D0	External DRAM-data
42	D2	External DRAM-data
43	D3	External DRAM-data
44	VSS4	0 V digital supply
45	CASQ	Column address strobe
46	N.C.	Not connected
47	N.C.	Not connected
48	N.C.	Not connected
49	VSS3	0 V digital supply
50	N.C.	Not connected
51	N.C.	Not connected
52	N.C.	Not connected
53	N.C.	Not connected
54	N.C.	Not connected
55	VSS2	0 V digital supply
56	VBB	Substrate bias voltage N.C.* (depends on version)
57	N.C.	Not connected

58	VSSA2	Analog ground
59	RGB-GND	RGB-ground
60	VSS1	0 V digital supply
61	R	Analog red display output
62	G	Analog green display output
63	B	Analog blue display output
64	BLAN	Blanking signal open drain output
65	CORQ	Contrast reduction open drain output
66	SCL	Bi-directional I^2C Bus clock port
67	SDA	Bi-directional I^2C Bus data port
68	I^2CEN	I^2C Bus enable

14.5.DRAM 4MX4

14.5.1.General Description

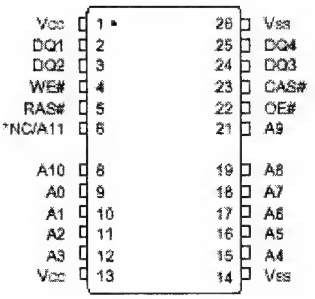
The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 con-figuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address (the latter 11 bits for 2K and the latter 10 bits for 4K, address pins A10 and A11 are "don't care"). READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data outputs will drive read data from the accessed location. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

14.5.2.Features

- Industry-standard x4 pin out, timing, functions and packages
- State-of-the-art, high-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or +5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE- RAS# (CBR)
- Optional Self Refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access cycle
- 5V-tolerant inputs and I/Os on 3.3V devices

14.5.3.Pin Assignment

24/26-Pin SOJ
(DA-2)



Top View

*NC on 2K refresh and A11 on 4K refresh options. **Note:** The "#" symbol indicates signal is active LOW.

14.6.SDA9400

14.6.1.General Description

The SDA9400 is a new component of the Micronas MEGAVISION ® IC set in a 0.35µm embedded DRAM technology (frame memory embedded). The SDA9400 is pin compatible to the SDA9401 (field memory embedded). The SDA9400 comprises all main functionalities of a digital feature box in one monolithic IC. The scan rate conversion to 100/120 Hz interlaced (50/60 Hz progressive) is based on a motion adaptive algorithm. The scan rate converted picture can be vertically expanded. The SDA9400 has a free running mode, therefore features like scan rate conversion to e.g. 70, 75 Hz with joint lines or multiple picture display (e.g. tuner scan) are possible. Due to the frame based signal processing, the noise reduction has been greatly improved. Furthermore separate motion detectors for luminance and chrominance have been implemented. For automatic controlling of the noise reduction parameters a noise measurement algorithm is included, which measures the noise level in the picture or in the blanking period. In addition a spatial noise reduction is implemented, which reduces the noise even in the case of motion. The input signal can be compressed horizontally and vertically with a certain number of factors. Therefore split screen is supported. Beside these additional functions like coloured background, windowing and flashing are implemented.

14.6.2.Features

• Two input data formats
- 4:2:2 luminance and chrominance parallel (2 x 8 wires)
- ITU-R 656 data format (8 wires)

• Two different representations of input chrominance data
- 2's complement code
- Positive dual code

• Flexible input sync controller

• Flexible compression of the input signal
- Digital vertical compression of the input signal (1.0, 1.25, 1.5, 1.75, 2.0, 3.0, 4.0)
- Digital horizontal compression of the input signal (1.0, 2.0, 4.0)

• Noise reduction
- Motion adaptive spatial and temporal noise reduction (3D-NR)
- Temporal noise reduction for luminance frame based or field based
- Temporal noise reduction for chrominance field based
- Separate motion detectors for luminance and chrominance
- Flexible programming of the temporal noise reduction parameters
- Automatic measurement of the noise level (5-bit value, readable by I²C bus)

• 3-D motion detection
- High performance motion detector for scan rate conversion
- Global motion detection flag (readable by I²C bus)
- Movie mode and phase detector (readable by I²C bus)

• TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)

• Embedded memory
- 5 Mbit embedded DRAM core for field memories
- 192 kbit embedded DRAM core for line memories

• Flexible clock and synchronization concept
- Decoupling of the input and output clock system possible

• Scan rate conversion
- Motion adaptive 100/120 Hz interlaced scan conversion
- Motion adaptive 50/60 Hz progressive scan conversion
- Simple static interlaced and progressive conversion modes for 100/120 Hz interlaced or 50/60 Hz progressive scan conversion: e.g. ABAB, AABB, AA*B*B, AAAA, BBBB, AB, AA*
- Simple progressive scan conversion with joint lines:
50 Hz -> 60, 70, 75 Hz progressive
60 Hz -> 70, 75 Hz progressive
- Large area and line flicker reduction

• Flexible digital vertical expansion of the output signal (1.0, ... [1/32] ..., 2.0)

• Flexible output sync controller
- Flexible positioning of the output signal
- Flexible programming of the output sync raster
- External synchronization by backend IC possible
(e.g. split screen for one TV channel with joint lines and one PC VGA channel)

• **Signal manipulations**
- Insertion of coloured background
- Vertical and/or horizontal windowing with four different speed factors
- Flash generation (for supervising applications, motion flag readable by I²C bus)
- Still frame or field
- Support of split screen applications
- Multiple picture display - Tuner scan (4 and 16 times for 4:3, 12 times for 16:9 tubes)
- Support of multi picture display with PIP or front-end processor with integrated scaler
(e.g. 9 times display of PIP pictures, picture tracking, random pictures, still-in-moving picture, moving-in-still picture)
• I²C-bus control (400 kHz)
• P-MQFP-64 package
• 3.3 V ± 5% supply voltage

14.6.3.Pin Definition

Pin No.	Name	Type	Description
2,8,24,42,55	VSS1	S	Supply voltage (*V* SS = 0 V)
9,25,41,56	VDD1	S	Supply voltage (*V* DD = 3.3 V)
36,52,58	VSS2	S	Supply voltage (*V* SS = 0 V)
35,51,53,57,59	VDD2	S	Supply voltage (*V* DD = 3.3 V)
43,..,50	YIN0...7	I/TTL	Data input Y (see input data format)
31,..,34;37,...,40	UVIN0...7	I/TTL PD	Data input UV (for 4:2:2 parallel, see input data format) (for CCIR 656, see input data format)
30	RESET	I/TTL	System reset. The RESET input is low active. In order to ensure correct operation a "Power On Reset" must be performed. The RESET pulse must have a minimum duration of two clock periods of the system clock CLK1.
23	HIN	I/TTL PD	H-Sync input (only for full CCIR 656)
22	VIN	I/TTL PD	V-Sync input (only for full CCIR 656)
29	SYNCEN	I/TTL	Synchronization enable input
21	SDA	I/O	I²C-Bus data line (5V ability)
20	SCL I	I	I²C-Bus clock line (5V ability)
54	CLK1	I/TTL	System clock 1
17,..,10	UVOUT0...7	O/TTL	Data output UV (see output data format)
7,..,3;1;64;63	YOUT0...7	O/TTL	Data output Y (see output data format)
62	HREF	O/TTL	Horizontal active video output
61	VOUT/ VEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): V-Sync output EXSYN=1: External V-Sync input for output part
60	HOUT/ HEXT	I/O/ TTL	EXSYN=0 (I²C-bus parameter): H-Sync output EXSYN=1: External H-Sync input for output part
18	INTERLACED	O/TTL	Interlace signal for AC coupled vertical deflection
28	X1 / CLK2	I/TTL	Crystal connection / System clock 2
27	X2	O/AN	Crystal connection
26	CLKOUT	O/TTL	Clock output (depends on I²C parameters CLK11EN, CLK21EN, FREQR)
19	TEST	I/TTL	Test input, connect to *V* SS for normal operation

14.7.LM317T

14.7.1.Description

The LM317T is an adjustable 3 terminal positive voltage regulator capable of supplying in excess of 1.5 amps over an output range of 1.25 to 37 volts. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof. The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

14.7.2.Features

• Output Current in Excess of 1.5 A

• Output Adjustable between 1.2 V and 37 V
• Internal Thermal Overload Protection
• Internal Short Circuit Current Limiting Constant with Temperature
• Output Transistor Safe–Area Compensation
• Floating Operation for High Voltage Applications
• Available in Surface Mount D^2PAK, and Standard 3–Lead Transistor Package
• Eliminates Stocking many Fixed Voltages

14.8.DDP3310

14.8.1.Description

The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-end applications in 100/120-Hz TV sets with 4:3 or 16:9 picture tubes. The IC can be combined with members of the DIGIT 3000 IC family (VPC 32xx, TPU 3040), or it can be used with third-party products. The IC contains the entire digital video component and deflection processing and all analog interface components.

14.8.2.Features

Video processing
– linear horizontal scaling (0.25 ... 4)
– non-linear horizontal scaling "panorama-vision"
– dynamic peaking
– soft limiter (gamma correction)
– color transient improvement
– programmable RGB matrix
– picture frame generator
– two analog RGB/Fast-Blank inputs. The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-

Deflection processing
– scan velocity modulation output
– high-performance H/V deflection
– EHT compensation for vertical / East/West
– soft start/stop of H-Drive
– vertical angle and bow
– differential vertical output
– vertical zoom via deflection
– horizontal and vertical protection circuit
– adjustable horizontal frequency for VGA/SVGA display

Miscellaneous
– selectable 4:1:1/ 4:2:2 YC $_r$ C $_b$ input
– selectable 27/ 32-MHz line-locked clock input
– crystal oscillator for horizontal protection
– automatic picture tube adjustment (cutoff, white-drive)
– single 5-V power supply
– hardware for simple 50/60-Hz to 100/ 120-Hz conversion (display frequency doubling)
– two I^2C-controlled PWM outputs
– beam current limiter

14.8.3.Pin connection and short descriptions

NC = not connected
X = obligatory; connect as described in circuit diagram
OUT = Output
LV = if not used, leave vacant
IN = Input
SUPPLY = Supply Pin

Pin no PLCCK 68 pin	Pin name	Type	Connection (if not used)	Short description
1	VSUPP	SUPPLY	X	Supply voltage, Output pin driver
2	GNDP	SUPPLY	X	Ground, Output pin driver
3	VS2	IN	GNDD	Additional VSYNC input
4	FIFORRD	OUT	LV	FIFO Read counter reset

5	FIFORD	OUT	LV	FIFO Read Enable
6	FIFOWR	OUT	LV	FIFO Write Enable
7	FIFORWR	OUT	LV	FIFO Write counter reset
8	HOUT	OUT	X	Horizontal Drive Output
9	HFLB	IN	Hout	Horizontal Flyback Input
10	SAFETY	IN	GNDO	Safety Input
11	VPROT	IN	GNDO	Vertical protection Input
12	FREQSEL	IN	X	Selection of H-Drive Frequency Range
13	CM1	IN	X	Clock select 40.5 or 27/32 MHz
14	CMO	IN	X	Clock select 27/32 MHz
15	RSW2	OUT	LV	Range Switch2, Measurement ADC
16	RSW1	IN/OUT	LV	Range Switch1, Measurement ADC
17	SENSE	IN	GNDO	Sense ADC Input
18	GNDM	SUPPLY	X	Ground, MADC Input
19	VERT+	OUT	GNDO	Differantial Vertical Sawtooth Output
20	VERT-	OUT	GNDO	Differantial Vertical Sawtooth Output
21	EW	OUT	GNDO	Vertical Parabola Output
22	XREF	IN	X	Reference Input for RGB DACs
23	SVM	OUT	VSUPO	Scan Velocity Modulation
24	ROUT	OUT	VSUPO	Analog Output Red
25	GOUT	OUT	VSUPO	Analog Output Green
26	BOUT	OUT	VSUPO	Analog Output Blue
27	GNDO	SUPPLY	X	Ground, Analog Back-end
28	VSUPO	SUPPLY	X	Supply Voltage, Analog Back-end
29	VRD/BCS	IN	X	DAC Reference, Beam Current Safety
30	FBLIN1	IN	GNDO	Fast-Blank1 Input
31	RIN1	IN	GNDO	Analog Red1 Input
32	GIN1	IN	GNDO	Analog Green1 Input
33	BIN1	IN	GNDO	Analog Blue1 Input
34	FBLIN2	IN	GNDO	Fast-Blank2 Input
35	RIN2	IN	GNDO	Analog Red2 Input
36	GIN2	IN	GNDO	Analog Green2 Input
37	BIN2	IN	GNDO	Analog Blue2 Input
38	TEST	IN	GNDD	Test Pin
39	RESQ	IN	X	Reset Input, active low
40	PWM1	OUT	LV	I^2C-controlled DAC
41	PWM2	OUT	LV	I^2C-controlled DAC
42	HCS	IN	GNDD	Half-contrast
43	C0	IN	GNDD	Picture Bas Chroma (LSB)
44	C1	IN	GNDD	Picture Bas Chroma
45	C2	IN	GNDD	Picture Bas Chroma
46	C3	IN	GNDD	Picture Bas Chroma
47	C4	IN	GNDD	Picture Bas Chroma
48	C5	IN	GNDD	Picture Bas Chroma
49	C6	IN	GNDD	Picture Bas Chroma
50	C7	IN	GNDD	Picture Bas Chroma (MSB)
51	VSUPD	SUPPLY	X	Supply Voltage, Digital Circuitry
52	GNDD	SUPPLY	X	Ground, Digital Circuitry
53	LLC2	IN	X	System Clock Input (27/32/40.5 MHz)
54	Y0	IN	GNDD	Picture Bas Luma (LSB)
55	Y1	IN	GNDD	Picture Bas Luma
56	Y2	IN	GNDD	Picture Bas Luma
57	Y3	IN	GNDD	Picture Bas Luma
58	Y4	IN	GNDD	Picture Bas Luma
59	Y5	IN	GNDD	Picture Bas Luma
60	Y6	IN	GNDD	Picture Bas Luma
61	Y7	IN	GNDD	Picture Bas Luma (MSB)
62	LLC1	IN	VSUPD	Single Line-Locked Clock Input (13.5/16 MHz)
63	HS	IN	X	Horizontal Sync Input
64	VS	IN	GNDD	Vertical Sync Input
65	XTALK2	OUT	X	Analog Crystal Output (5-MHz Security Clock)
66	XTALK1	IN	X	Analog Crystal Input (5-MHz Security Clock)
67	SDA	IN/OUT	X	I^2C-Bus Data
68	SCL	IN/OUT	X	I^2C-Bus Clock

14.9.SDA5550

14.9.1.General definition

The SDA5550M is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to 17 Kbytes. This device can support external memory up to 1Mbyte ROM and RAM.TVTEXT Controller contains a data slicer for VPS, WSS, PDC and TXT, an acceleration acquisition hardware module, a display generator for Level 1.5 TXT and powerful On screen Display capabilities based on parallel attributes, and pixel oriented characters (DRCS). The 8 bit Microcontroller operates at 360nsec cycle time (min). Controller with dedicated hardware does most of the internal TXT acquisition processing, transfer data to/from external memory interface and receives/transmits data via I^2C-firmware user interface. SDA5550M is realized in 0.25 micron technology with 2.5V supply voltage and 3.3V I/O compatible. The IC produces the following input or output control signals; AGC_CON, MODE_SW, L / L', PIP_MODS, PIP_SEL, ON/OFF (stand-by), SC1..3_IN_AV (pin 8 information from 3 SCARTs), AFC, MUTE (to mute audio output IC), I^2CEN.

14.9.2.Features

General

- Feature selection via special function register
- Simultaneous reception of TTX, VPS, PDC, and WSS (line 23)
- Supply Voltage 2.5 and 3.3 V

External Crystal and Programmable clock speed

Single external 6MHz crystal, all necessary clocks are generated internally
CPU clock speed selectable via special function registers.
Normal Mode 33.33 MHz CPU clock, Power Save mode 8.33 MHz

Microcontroller Features

- 8bit 8051 instruction set compatible CPU.
- 33.33-MHz internal clock (max.)
- 0.360ms (min.) instruction cycle
- Two 16-bit timers
- Watchdog timer
- Capture compare timer for infrared remote control decoding
- Pulse width modulation unit (2 channels 14 bit, 6 channels 8 bit)
- ADC (4 channels, 8 bit)
- UART

Memory

- Non-multiplexed 8-bit data and 16 ... 20-bit address bus (ROMless Version)
- Memory banking up to 1Mbyte (Romless version)
- Up to 128 Kilobyte on Chip Program ROM
- Eight 16-bit data pointer registers (DPTR)
- 256-bytes on-chip Processor Internal RAM (IRAM)
- 128bytes extended stack memory.
- Display RAM and TXT/VPS/PDC/WSS-Acquisition-Buffer directly accessible via MOVX
- UP to 16KByte on Chip Extended RAM (XRAM) consisting of;
- 1 Kilobyte on-chip ACQ-buffer-RAM (access via MOVX)
- 1 Kilobyte on-chip extended-RAM (XRAM, access via MOVX) for user software
- 3 Kilobyte Display Memory

Display Features

- ROM Character Set Supports all East and West European Languages in single device
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters

• Variable Flash Rate
• Programmable Screen Size (25 Rows x 33...64 Columns)
• Flexible Character Matrixes (HxV) 12 x 9...16
• Up to 256 Dynamical Redefinable Characters in standard mode; 1024 Dynamical Redefinable Characters in Enhanced Mode
• CLUT with up to 4096 color combinations
• Up to 16 Colors per DRCS Character
• One out of Eight Colors for Foreground and Background Colors for 1-bit DRCS and ROM Characters
• Shadowing
• Contrast Reduction
• Pixel by Pixel Shiftable Cursor With up to 4 Different Colors
• Support of Progressive Scan and 100 Hz.
• 3 X 4Bits RGB-DACs On-Chip
• Free Programmable Pixel Clock from 10 MHz to 32MHz
• Pixel Clock Independent from CPU Clock
• Multinorm H/V-Display Synchronization in Master or Slave Mode

Acquisition Features
• Multistandard Digital Data Slicer
• Parallel Multi-norm Slicing (TTX, VPS, WSS, CC, G+)
• Four Different Framing Codes Available
• Data Caption only Limited by available Memory
• Programmable VBI-buffer
• Full Channel Data Slicing Supported
• Fully Digital Signal Processing
• Noise Measurement and Controlled Noise Compensation
• Attenuation Measurement and Compensation
• Group Delay Measurement and Compensation
• Exact Decoding of Echo Disturbed Signals

Ports
• One 8-bit I/O-port with open drain output and optional I^2C Bus emulation support (Port 0)
• Two 8-bit multifunction I/O-ports (Port 1, Port 3)
• One 4-bit port working as digital or analog inputs for the ADC (Port 2)
• One 2-bit I/O port with secondary functions (P4.2, 4.3, 4.7)
• One 4-bit I/O-port with secondary function (P4.0, 4.1, 4.4) (Not available in P-SDIP 52)

14.10.TEA6415C

14.10.1.General Description

The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75? load needs an external transistor. It is possible to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

14.10.2.Features

• 20MHz Bandwidth
• Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
• 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
• 6 Outputs
• Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
• Bus controlled
• 6.5dB gain between any input and output
• 55dB crosstalk at 5mHz

• Fully ESD protected

14.10.3.Pinning

1.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
2.	Data	:	Low level : -0.3V Max: 1.5V,
			High level : 3.0V Max : Vcc+0.5V
3.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA
4.	Clock	:	Low level : -0.3V Max: 1.5V,
			High level : 3.0V Max : Vcc+0.5V
5.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
6.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
7.	Prog		
8.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
9.	Vcc	:	12V
10.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
11.	Input	:	Max : 2Vpp, Input Current: 1mA, Max: 3mA
12.	Ground		
13.	Output	:	5.5Vpp, Min : 4.5Vpp
14.	Output	:	5.5Vpp, Min : 4.5Vpp
15.	Output	:	5.5Vpp, Min : 4.5Vpp
16.	Output	:	5.5Vpp, Min : 4.5Vpp
17.	Output	:	5.5Vpp, Min : 4.5Vpp
18.	Output	:	5.5Vpp, Min : 4.5Vpp
19.	Ground		
20.	Input	:	Max : 2Vpp, Input Current: 1mA, Max : 3mA

14.11.VPC3230D

14.11.1.General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products. The main features of the VPC 323xD are;
– high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
– multi-standard color decoder PAL/NTSC/SECAM including all substandards
– four CVBS, one S-VHS input, one CVBS output
– two RGB/YC r C b component inputs, one Fast Blank (FB) input
– integrated high-quality A/D converters and associated clamp and AGC circuits
– multi-standard sync processing
– linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panorama-vision'
– PAL+ preprocessing
– line-locked clock, data and sync, or 656-output interface
– peaking, contrast, brightness, color saturation and tint for RGB/ YC r C b and CVBS/ S-VHS
– high-quality soft mixer controlled by Fast Blank
– PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
– 15 predefined PIP display configurations and expert mode (fully programmable)
– control interface for external field memory
– I^2C-bus interface
– one 20.25-MHz crystal, few external components
– 80-pin PQFP package

14.11.2.Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input

3	R1/CR1IN	IN	VREF	Read1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Read2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
8	FFRSTWIN	IN	LV or GND_D	FIFO Reset Write Input
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^2C Bus Clock
14	SDA	IN/OUT	X	I^2C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	GND_D	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock output 20.25 MHz
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front End/Back-End Data/Front-End Vertical Sync Output
59	V_{STBYY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
61	NC	-	LV or GND_D	Not Connected
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog

67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV	Chroma/Analog Video 5 Input
72	VIN1	IN	VRT	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}

14.12.TDA1308T

14.12.1.General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications. It gets its input from two analog audio outputs (DACA_L and DACA_R) of MSP3411G. The gain of the output is adjustable by the feedback resistor between the inputs and outputs.

14.12.2.Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- high signal-to-noise ratio
- High slew rate
- Low distortion
- Large output voltage swing.

14.12.3.Pinning

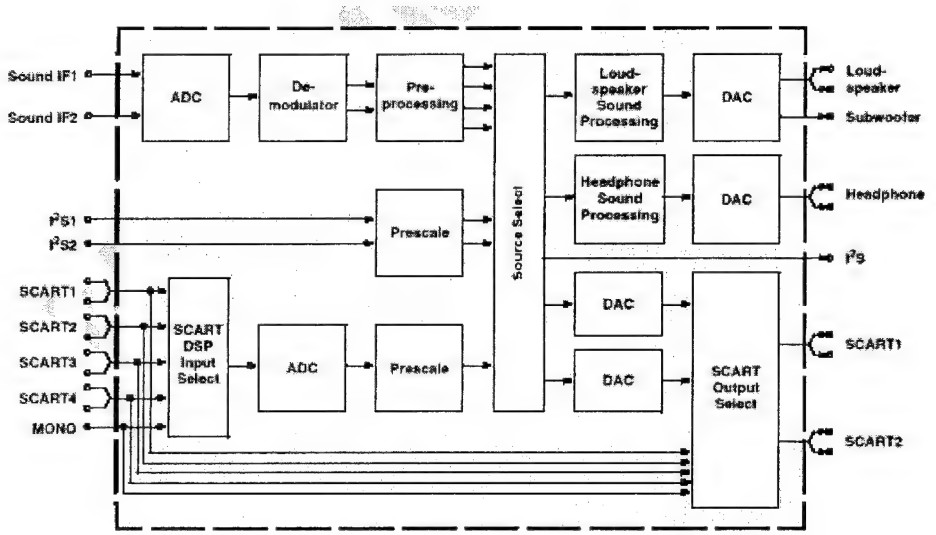
SYMBOL	PIN	DESCRIPTION
OUTA	1	Output A
INA(neg)	2	Inverting input A
INA(pos)	3	Non-inverting input A
V_{SS}	4	Negative supply
INB(pos)	5	Non-inverting input B
INB(neg)	6	Inverting input B
OUTB	7	Output B
V_{DD}	8	Positive supply

14.13.MSP34X1G (MSP3411G)

14.13.1.Description

The MSP 34x1G family of single-chip Mullet-standard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP34x1G. The MSP34x1G has all functions of the MSP34x0G with the addition of a virtual surround sound feature. Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP34x1G includes our virtualizer algorithm "3D-PANORAMA" which has been approved by the Dolby 1) Laboratories for compliance with the "Virtual Dolby Surround" technology. In addition, the MSP34x1G includes the

"PANORAMA" algorithm. These TV sound processing ICs include versions for processing the multi-channel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP34x1G has optimum stereo performance without any adjustments. All MSP 34xxG versions are pin and software downward compatible to the MSP 34xxD. MSP34x1G further simplifies controlling software. Standard selection requires a single I^2C transmission only. The MSP34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).



14.13.2.Features

3D-PANORAMA virtualizer (approved by Dolby Laboratories) with noise generator
PANORAMA virtualizer algorithm
Standard Selection with single I^2C transmission
Automatic Standard Detection of terrestrial TV standards/Automatic Carrier Mute function
Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
Two selectable sound IF (SIF) inputs
Interrupt output programmable (indicating status change)
Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
Loudspeaker channel with MDB (Micronas Dynamic Bass)
AVC: Automatic Volume Correction
Subwoofer output with programmable low-pass and complementary high-pass filter
5-band graphic equalizer for loudspeaker channel
Spatial effect for loudspeaker channel; processing of all deemphasis filtering
Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs
Complete SCART in/out switching matrix
Two I^2S inputs; one I^2S output
All analog FM-Stereo A2 and satellite standards
All analog Mono sound carriers including AM-SECAM L
Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
ASTRA Digital Radio (ADR) together with DRP 3510A
All NICAM standards
Korean FM-Stereo A2 standard

14.13.3.Pin connections

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	-	-	-	-	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR Data Output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I^2S data output
6	12	10	5	4	I2S_WS	IN/OUT	LV	I^2S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I^2S clock
8	10	8	3	2	I2C_DA	IN/OUT	X	I^2C data
9	9	7	2	1	I2C_CL	IN/OUT	X	I^2C data
10	8	-	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	X	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	X	I^2C bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	-	76	59	NC		LV	Not connected
16	2	-	75	58	NC		LV	Not connected
17	-	-	-	-	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	53	TESTEN	IN	X	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF/LV	IF Input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN-	IN	AVSS via 56 pF/LV	IF common (can be left vacant, only if IF input 1 is also not in use)
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 2
26	57	46	66	49	AVSUP		X	Analog power supply 5v
-	-	-	65	-	AVSUP		X	Analog power supply 5v
-	-	-	64	-	NC		LV	Not connected
-	-	-	63	48	NC		LV	Not connected
27	56	45	62	48	AVSS		X	Analog ground
-	-	-	61	-	AVSS		X	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
-	-	-	59	-	NC		LV	Not connected
29	54	43	58	46	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	-	55	43	ASG		AHVSS	Analog Shield Ground
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	-	52	40	ASG		AHVSS	Analog Shield Ground
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right
37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	-	49	37	ASG		AHVSS	Analog Shield Ground
39	44	-	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	-	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	-	-	46	-	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		X	Analog reference voltage
43	41	35	44	33	AHVSS		X	Analog ground
-	-	-	43	-	AHVSS		X	Analog ground
-	-	-	42	-	NC		LV	Not connected
-	-	-	41	-	NC		LV	Not connected
44	40	34	40	32	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		X	Analog power supply 8V

46	38	32	38	30	CAPL_A		X	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF		X	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	-	-	32	-	NC		LV	Not connected
53	32	-	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output
55	30	-	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		X	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
-	-	-	23	-	NC		LV	Not connected
-	-	-	22	-	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	X	Power-on-reset
62	23	-	20	15	NC		LV	Not connected
63	22	-	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I^2S2-data input
66	19	17	16	11	DVSS		X	Digital ground
-	-	-	15	-	DVSS		X	Digital ground
-	-	-	14	-	DVSS		X	Digital ground
67	18	16	13	10	DVSUP		X	Digital power supply 5V
-	-	-	12	-	DVSUP		X	Digital power supply 5V
-	-	-	11	-	DVSUP		X	Digital power supply 5V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

14.14.TL431

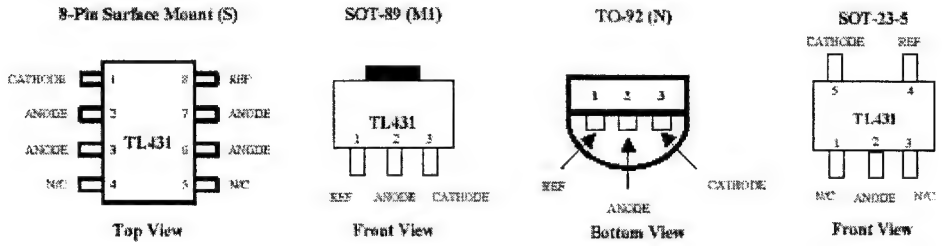
14.14.1.Description

The TL431 is a 3-terminal adjustable shunt voltage regulator providing a highly accurate 1 % band gap reference. TL431 acts as an open-loop error amplifier with a 2.5V temperature compensation reference. The TL431 thermal stability, wide operating current (150mA) and temperature range (0.to 105.makes it suitable for all variety of application that are looking for a low cost solution with high performance. The output voltage may be adjusted to any value between VREF and 36 volts with two external resistors. The TL431 is operating in full industrial temperature range of 0°C to 105°C. The TL431 is available in TO-92, SO-8, SOT-89 and SOT23-5 packages.

14.14.2.Features

- Trimmed Band gap to 1%
- Wide Operating Current 1mA to 150mA
- Extended Temperature Range 0. °C to 105.°C
- Low Temperature Coefficient 30 ppm /°C
- Offered in TO-92, SOIC, SOT-89, SOT-23-5
- Improved Replacement in Performance for TL431
- Low Cost Solution

14.14.3.Pin Configurations



14.15.DRX3960A

14.15.1.Introduction

The Digital Receiver Front-end DRX 3960A performs the entire multi-standard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF) with only one SAW filter. The IC is designed for applications in TV sets, VCRs, PC cards, and TV tuners. The alignment-free DRX 3960A needs no special external components. All control functions and status registers are accessible via I^2C bus interface. Therefore, it simplifies the design of high-quality, highly standardized IF stages. Due to its mixed signal structure and the digital demodulation, the IC offers unique features and is prepared for digital TV.

14.15.2.Features

– Multi-standard QSS IF processing with a single SAW
– Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)
– Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 36.125 MHz etc.)
– Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
– Standard specific digital post filtering
– Standard specific digital video/audio splitting
– Standard specific digital picture carrier recovery:
– alignment-free
– Quartz-stable and accurate
– Stable frequency lock at 100% modulation and over modulation up to 115%
– Quartz-accurate AFC information
– Programmable standard specific digital group delay equalizing
– Automatically frequency-adjusted Nyquist slope, therefore optimal picture and sound performance over complete lock in frequency range
– Standard specific digital AGC and delayed tuner AGC with programmable tuner Take Over Point
– Fast AGC due to linear structure
– Adaptive back porch control, therefore fast positive modulation AGC
– No sound traps needed at video output
– Second SIF output with standard dependent pre-filtering and amplitude controlled output level
– Optimal sound SNR due to carrier recovery without quadrature distortions
– FM radio capability without external components and with standard TV tuner
– Prepared for digital TV (DVB-C, DVB-T, ATSC)
– I^2C bus interface

14.15.3.Pin connection and short descriptions

NC = not connected, leave vacant
DVSS = if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram

LV = if not used, leave vacant
AHVSS = connect to AHVSS

Pin no PLCCK 68 pin	Pin name	Type	Supply Voltage	Connection (if not used)	Short description
1	AVSS_ADC			X	Analog Ground for ADC
2	AVDD_ADC			X	Analog Supply for ADC (+5V)
3	ANASTX	I/O	AVDD_FE8	GND	Test pin
4	ANASTY	I/O	AVDD_FE8	GND	Test pin
5	AVDD_FE8			X	2nd analog supply for the front-end
6	AVSS_FE8			X	2nd analog ground for the front-end
7	AVSS_FE40				1st analog ground for the front-end
8	IFINX	IN	AVDD_FE40	X	IF Input
9	AVDD_FE40			X	1st analog supply for the front-end
10	IFINY	IN	AVDD_FE40	X	IF Input
11	AVSS_FE40			X	1st analog ground for the front-end
12	AVDD_SYN			X	Analog supply for synthesizer (+5V)
13	AVSS_SYN			X	Analog ground for synthesizer
14	SHIELD	IN		X	Shield GND
15	TEST0	IN	AVDD_DAC	GND	Test pin
16	TEST1	IN	AVDD_DAC	GND	Test pin
17	TEST2	IN	AVDD_DAC	GND	Test pin

18	CVBS	OUT	AVDD_DAC	X	CVBS Output
19	REF_SW	IN	AVDD_DAC	X	Reference frequency switch
20	SIF	OUT	AVDD_DAC	X	2nd SIF output
21	AVDD_DAC			X	DAC supply (+5V)
22	AVSS_DAC			X	DAC ground
23	TEST_EN	IN	DVDD	GND	Test enable
24	RESETQ	IN	DVDD	X	Reset
25	I2C_SDC	I/O	DVDD	X	I^2C data
26	I2C_SCL	I/O	DVDD	X	I^2C clock
27	DVDD_CAP			X	Digital supply capacitor
28	DVDD			X	Digital supply (+3.3V)
29	DVSS			X	Digital ground
30	DVSS_CAP			X	Digital capacitor ground
31	PORT0	OUT	DVDD	LV	Digital output port
32	PORT1	OUT	DVDD	LV	Digital output port
33	TUNER_AGC	OUT	DVDD	X	Tuner AGC current output
34	PORT2	OUT	DVDD	LV	Digital output port
35	PORT3	OUT	DVDD	LV	Digital output port
36	PORT4	OUT	DVDD	LV	Digital output port
37	ADR_SEL	IN	DVDD	X	Address select
38	PORT5	OUT	DVDD	LV	Digital output port
39	DVDD_ADC			X	Digital supply for ADC (+3.3V)
40	DVSS_ADC			X	Digital ground for ADC
41	XTAL_IN	IN	AVDD_ADC	X	Crystal oscillator
42	XTAL_OUT	I/O	AVDD_ADC	X	Crystal oscillator/external reference frequency
43	VREF		AVDD_ADC	X	ADC Reference voltage
44	SGND		AVDD_ADC	X	ADC Reference ground

14.16.LM7808

14.16.1.Description

The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D 2 PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shutdown and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

14.16.2.Features

Output Current Up To 1.5 A
Output Voltages of 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
Thermal Over load protection
Short Circuit Protection
Output Transition SOA Protection

14.17.BDX53BFI

14.17.1.Description

The BDX53BFI is silicon epitaxial-base NPN power transistor in monolithic Darlington configuration and are mounted in ISOWATT220 plastic package. It is intended for use in hammer drivers, audio amplifiers and other medium power linear and switching applications. The complementary PNP type is the BDX54BFI.

14.17.2.Applications

General purpose switching and amplifier
Linear and switching industrial equipment

14.18.TDA8177F

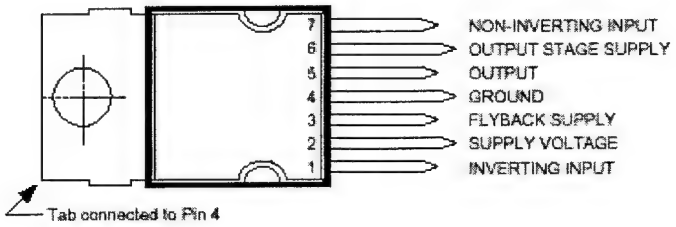
14.18.1.Description

Designed for monitors and high performance TVs, the TDA8177F vertical deflection booster can handle flyback voltage up to 70V. More than this it is possible to have a flyback voltage, which is more than the double of the supply (Pin 2). This allows to decrease the power consumption or to decrease the flyback time for a given supply voltage. The TDA8177F operates with supplies up to 35V and provides up to 3APP output current to drive the yoke.

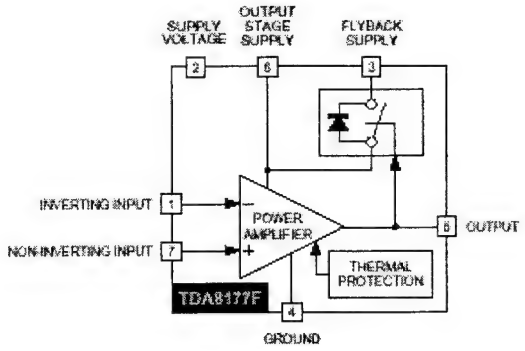
14.18.2.Features

Power Amplifier
Thermal Protection
Output Current Up To 3.0APP
Flyback Voltage Up To 70V (on Pin 5)
Suitable For Dc Coupling Application
External Flyback Supply

14.18.3.Pin connections



14.18.4.Block Diagram



14.19.LM1086

14.19.1.Description

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in five fixed voltages: 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors. The LM1086 circuit includes a zener trimmed band-gap reference, current limiting and thermal shutdown.

14.19.2.Features

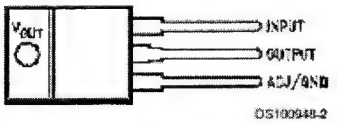
Available in 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
Current Limiting and Thermal Protection

Output Current 1.5A
Line Regulation 0.015% (typical)
Load Regulation 0.1% (typical)

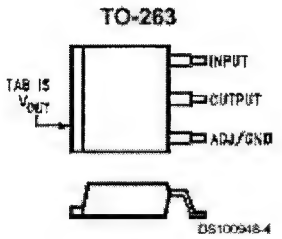
14.19.3.Applications

SCSI-2 Active Terminator
High Efficiency Linear Regulators
Battery Charger
Post Regulation for Switching Supplies
Constant Current Regulator
Microprocessor Supply

14.19.4.Connection Diagrams



Top View



Top View

14.20.MC44608

14.20.1.Description

The MC44608 is a high performance voltage mode controller designed for off–line converters. This high voltage circuit that integrates the start–up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability. The device also features a very high efficiency stand–by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand–by power consumption to approximately 1W while delivering 300mW in a 150W SMPS.

- Integrated Start–Up Current Source
- Lossless Off–Line Start–Up
- Direct Off–Line Operation
- Fast Start–Up

14.20.2.General Features

- Flexibility
- Duty Cycle Control
- Under voltage Lockout with Hysteresis
- On Chip Oscillator Switching Frequency 40, or 75kHz
- Secondary Control with Few External Components

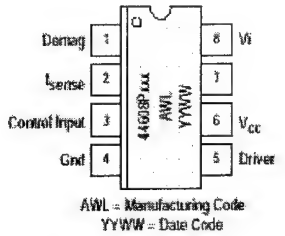
Protections

- Maximum Duty Cycle Limitation
- Cycle by Cycle Current Limitation
- Demagnetization (Zero Current Detection) Protection
- "Over Vcc Protection" Against Open Loop
- Programmable Low Inertia Over Voltage Protection Against Open Loop
- Internal Thermal Protection

GreenLine™ Controller

- Pulsed Mode Techniques for a Very High Efficiency Low Power Mode
- Lossless Startup
- Low dV/dT for Low EMI Radiations

14.20.3.Pin Connections



14.20.4.Pin Function description

Pin	Name	Description
1	Demag	The Demag pin offers 3 different functions: Zero voltage crossing detection (50mV), 24mA current detection and 120mA current detection. The 24mA level is used to detect the secondary reconfiguration status and the 120mA level to detect an Over Voltage status called Quick OVP.
2	ISENSE	The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the power MOSFET. When I sense reaches 1V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A 200mA current source is flowing out of the pin 3 during the start–up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 3; thus a programmable peak current detection can be performed during the SMPS stand–by mode.
3	Control Input	A feedback current from the secondary side of the SMPS via the opto–coupler is injected into this pin. A resistor can be connected between this pin and GND to allow the programming of the Burst duty cycle during the Stand–by mode.
4	Ground	This pin is the ground of the primary side of the SMPS.
5	Driver	The current and slew rate capability of this pin are suited to drive Power MOSFETs.
6	VCC	This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 15V and the operating range is between 6.6V and 13V. An intermediate voltage level of 10V creates a disabling condition called Latched Off phase.
7		This pin is to provide isolation between the Vi pin 8 and the VCC pin 6.
8	Vi	This pin can be directly connected to a 500V voltage source for start–up function of the IC. During the Start–up phase a 9 mA current source is internally delivered to the VCC pin 6 allowing a rapid charge of the VCC capacitor. As soon as the IC starts–up, this current source is disabled.

14.21.TCET1102G

14.21.1.Description

The TCET110/ TCET2100/ TCET4100 consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 4-lead up to 16-lead plastic dual inline package. The elements are mounted on one lead frame using a **coplanar technique**, providing a fixed distance between input and output for highest safety requirements.

14.21.2.Applications

Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):
For appl. class I – IV at mains voltage =300 V
For appl. class I – III at mains voltage =600 V
According to VDE 0884, table 2, suitable for: **Switch-mode power supplies, line receiver, computer peripheral interface, microprocessor system interface.**

14.21.3.Features

VDE 0884 related features:
Rated impulse voltage (transient overvoltage) V_{IOTM} = 8 kV peak
Isolation test voltage (partial discharge test voltage) V_{pd} = 1.6 kV
Rated isolation voltage (RMS includes DC) V_{IOWM} = 600 V $_{RMS}$ (848 V peak)
Rated recurring peak voltage (repetitive) V_{IORM} = 600 V $_{RMS}$

General features:
CTR offered in 9 groups
Isolation materials according to UL94-VO
Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
Climatic classification 55/100/21 (IEC 68 part 1)
Special construction: Therefore, extra low coupling capacity of typical 0.2pF, high **C**ommon **M**ode **R**ejection
Low temperature coefficient of CTR
G = Leadform 10.16 mm; provides creepage distance > 8 mm, for TCET2100/ TCET4100 optional; suffix letter 'G' is not marked on the optocoupler
Coupling System U

14.22.TDA7480L

14.22.1.Description

The TDA7480L is an audio class-D amplifier assembled in Power DIP package specially de-signed for high efficiency applications mainly for TV and Home Stereo sets.

14.22.2.Features

10W Output Power: R_L = 8Ω/4Ω; THD = 10%
High Frequency
No Heatsink
Split Supply
Overvoltage Protection
St-By And Mute Features
Short Circuit Protection
Thermal Overload Protection

14.22.3.Pin Functions

Number	Name	Function
1	$-V_{CC}$	NEGATIVE SUPPLY.
2	$-V_{CC}$	NEGATIVE SUPPLY.
3	$-V_{CC}$	NEGATIVE SUPPLY.
4	OUT	PWM OUTPUT
5	BOOTDIODE	BOOTSTRAP DIODE ANODE
6	BOOT	BOOTSTRAP CAPACITOR
7	NC	NOT CONNECTED
8	FEEDCAP	FEEDBACK INTEGRATING CAPACITANCE
9	FREQUENCY	SETTING FREQUENCY RESISTOR
10	SGN-GND	SIGNAL GROUND
11	IN	INPUT
12	ST-BY-MUTE	ST-BY/ MUTE CONTROL PIN
13	NC	NOT CONNECTED
14	$+V_{CC}$ SIGN	POSITIVE SIGNAL SUPPLY
15	V_{REG}	10V INTERNAL REGULATOR
16	$+V_{CC}$ POW	POSITIVE POWER SUPPLY
17	$-V_{CC}$	NEGATIVE SUPPLY (TO BE CONNECTED TO PIN 16 VIA C5)
18	$-V_{CC}$	NEGATIVE SUPPLY
19	$-V_{CC}$	NEGATIVE SUPPLY
20	$-V_{CC}$	NEGATIVE SUPPLY

14.23.SAA3010T

14.23.1.Description

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section "Keyboard operation".

14.23.2.Features

Low voltage requirement
Biphase transmission technique
Single pin oscillator
Test mode facility

14.23.3.Pinning

Pin	Mnemonic	Function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	sense mode selection input
3	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	Scan drivers
14	VSS	Ground (0V)
15-17	DR-2-DR0 (ODN)	Scan drivers
18	OSC (I)	Oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	Test point 1
21-27	X0-X6 (IPU)	Sense inputs from key matrix
28	VDD(I)	Voltage supply

Note:
(I): Input,
(IPU): input with p-channel pull-up transistor,
(ODN): output with open drain n-channel transistor
(OD3): output 3-state

15.AK52 CHASSIS MANUAL ADJUSTMENTS PROCEDURE

15.1.PRELIMINARY

Before starting with the alignment procedure, make sure that all the potentiometers on the chassis and also screen and focus pots are in the medium position.

15.2.SYSTEM VOLTAGE ADJUSTMENTS

Inputs AC power (220V 50Hz)
PAL B/G test pattern via RF
(PAL I test pattern for PAL I TV's, SECAM D/K pattern, SECAM L/L'/K' TVs.)
Outputs Digital voltmeter to anode of D110.
Display System voltage
Action Apply power. Check that the stand-by Led lights.
Select TV mode and tune to the applied test pattern via local test keyboard.
Chassis should start normally.
Adjust all analog controls (volume, bass, treble, brightness, contrast, colour) to minimum settings.
Adjust VR127 according to the following different type of CRTs.

SYSTEM VOLTAGE	TYPE OF CRT
135V±0.5V	PHILIPS A66EAK552X54
135V±0.5V	PHILIPS A66EAK071X54
135V±0.5V	VIDEOCOLOR A66ECY13X12
135V±0.5V	PHILIPS W66ESF002X44

15.3.AFC ADJUSTMENTS

Inputs AC power
38.9 Mhz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model (90dBmV) to Z403 SAW filter input terminals 1 and 2.
Outputs Digital voltmeter to AFC point (pin22 of IC401)
Display AFC Voltage.
Action Adjust VL401 for 2.5±0.1 Volts. TV should automatically tune to a station when search tuning is activated.

15.4.FOCUS ADJUSTMENTS

Inputs AC power
PAL B/G test pattern via RF input.
Outputs Picture tube drive.
Display Picture
Action Select TV mode and tune to the signal.
Adjust focus potantiometer (the upper pot on the rear side of the FBT transformer) for optimum focusing drive.

15.5.SCREEN ADJUSTMENTS

Inputs AC power
PAL B/G Colour Bar test pattern via RF
Outputs 1/100 Oscilloscope probe to RGB cathodes on CRT baseboard.
NOTE: Ground pin of probe will be connected to 1st pin (GND) of the CRT socket.
Display RGB ratio
Action Select PAL B/G Colour bar pattern using the local test keyboard and the user remote control unit.
Adjust all control functions (brightness, colour and contrast) to minimum settings.
Measure the most sensitive cathode
Adjust the screen potentiometer (lower pot on the rear side of FBT transformer) until cathode voltage becomes 150V.

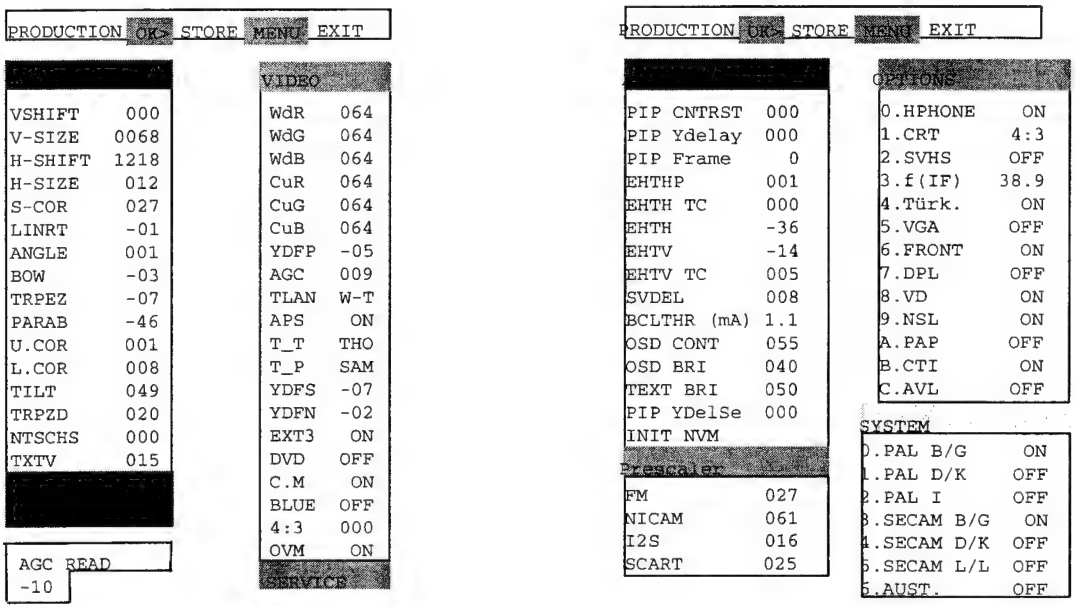
15.6.IF ADJUSTMENT FOR L' MODE

Inputs AC power
38.9 MHz test pattern for PAL B/G, PAL-SECAM B/G or 39.5 MHz test pattern for PAL I model. (90dBmV) to Z403 SAW filter input terminals 1 and 2.
Outputs Digital Voltmeter to AFC point. (pin22 of IC401)
Digital Voltmeter to AFC_L point. (pin14 of IC401
Display AFC Voltage.
Action Firstly adjust VL401 for 2.5±0.1 Volts. TV should automatically tune to a station when search tuning is activated.
Adjust VR401 for 2.5±0.1 Volts at the AFC_L point.

16.AK52 CHASSIS PRODUCTION SERVICE MODE ADJUSTMENTS

16.1.PRELIMINARY

All system, geometry and white balance alignments are performed in production service mode. Before starting the production mode alignments, make sure that all manual adjustments are done correctly. To start production mode alignments enter the MAIN MENU and then press the digits 1, 6, 7 and 5 respectively. The following first menu appears on the screen. Production mode values will appear on the screen.



First page

Second Page

SERVICE MENU

Production mode groups will be displayed with different colours of headlines, so in order to access a production alignment group press the colour button of the related group on the remote control transmitter.

- RED BUTTON is pressed to access H/V menu.
- GREEN BUTTON is pressed to access VIDEO adjust menu.
- BLUE BUTTON is pressed to go to the next page of the service menu.
- YELLOW BUTTON is used to adjust system parameters on the second page of the service menu.

After selecting one of the production service mode groups, you can access its items by pressing ? /? buttons. Selected parameter will be highlighted. Inorder to change the selected parameter, use ? /? buttons. Inorder to switch between other group of items press the colour key of this groups headline.
To store the settings press OK button. To exit the service menu press MENU button.
Entire service menu parameters of AK52 CHASSIS are listed below.

16.2.H/V (HORIZONTAL AND VERTICAL GEOMETRY ALIGNMENTS)

Switch the program to crosshatch test pattern. Press RED button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button. Switch the another parameter group by pressing the colour button of the related coloured headline of that group. Exit production mode by pressing the MENU button on the remote control.

V-SHIFT

Change Vertical Shift by pressing Left/Right buttons till the test pattern is vertically centered. Horizontal line at the center of the test pattern is in equal distance both to upper and lower side of the picture tube.

Check and readjust V-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	000

V-SIZE

Change Vertical Size by pressing Left/Right buttons till horizontal black lines on both the upper and lower part of the test pattern become very close to the upper and lower horizontal sides of picture tube and nearly about to disappear. Check and readjust V-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	068

H-SHIFT

Change Horizontal Shift by pressing Left/Right buttons till the the test pattern is horizontally in equal distance both to right and left sides of the picture tube. Check and readjust H-SHIFT item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	0000
Max. Value:	1295
Recommended Value:	1218

H-SIZE

Change Horizontal Size by pressing Left/Right buttons till no under-scan condition will happen, i.e. no white bars on the left and right side of the test pattern will be visible nor picture will be so wide. Check and readjust H-SIZE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	012

S-COR

Change S-Correction by pressing Left/Right buttons till the size of squares on both the upper and lower part of test pattern become equal to the squares laying on the vertical center of the test pattern. Check and readjust S-COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	027

LINRT

Change Linearity by pressing Left/Right buttons till all the size of squares of the test pattern become in equal size from the top of the screen to its bottom of the whole screen. Check and readjust LINRT item if the adjustment becomes improper after some other geometric adjustments are done. (especially after than S-COR adjustment)

Min. Value:	-128
Max. Value:	127
Recommended Value:	-01

ANGLE

Change Angle by pressing Left/Right buttons till the vertical lines of the crosshatch pattern become completely perpendicular to horizontal lines without any angle of vertical deviation. Check and readjust ANGLE item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	001

BOW
Change Bow by pressing Left/Right buttons till the vertical lines especially ones close to the left and right sides will of equal and symmetrical bending, i.e. they together will neither be towards left side nor right side. Check and readjust BOW item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-03

TRPEZ
Change Trapezium by pressing Left/Right buttons till vertical lines, especially lines at the sides of the picture frame became parallel to the both sides of picture tube as close as possible. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-07

PARAB
Change Parabol by pressing Left/Right buttons till vertical lines close to the both sides of the picture frame become parallel to vertical sides of picture tube without any bending to left or to right side of the screen. Check and readjust PARAB item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	-46

U.COR
Change Upper Correction by pressing Left/Right buttons till vertical lines at the upper corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust U.COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	001

L.COR
Change Lower Correction by pressing Left/Right buttons till vertical lines at the lower corners of the picture frame become vertical and parallel to vertical corner sides of picture tube. Check and readjust L.COR item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	-128
Max. Value:	127
Recommended Value:	008

TILT
This adjustment only works when the TV has rotation option. Change TILT by pressing Left/Right buttons to rotate the complete raster clock-wise and counter clock-wise depending on the CRT. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	000
Max. Value:	063
Recommended Value:	049

TRPZD
Not used for this model.

NTSCHS
Change NTSC horizontal size by pressing Left/Right buttons to adjust till no under-scan condition will happen, i.e. no white bars on the left and right side of the NTSC test pattern will be visible nor picture will be so wide. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.

Min. Value:	000
Max. Value:	010

Recommended Value: 000

TXTV
Change TXTV by pressing Left/Right buttons to adjust the proper vertical size of Teletext screen. Check and readjust TRPEZ item if the adjustment becomes improper after some other geometric adjustments are done.
Min. Value: 000
Max. Value: 040
Recommended Value: 015

16.3.VIDEO ALIGNMENTS
Switch the program to colour bar test pattern. Press GREEN button to access this group of item. Select the parameter by pressing up/down buttons. Adjust the parameter by pressing left/right buttons. Store the settings by pressing OK button.

WdR, WdG, WdB: WHITE BALANCE ADJUSTMENT
Apply WHITE test pattern via RF. Adjust all analog functions to medium level and set WdR to 86, WdG to 84, WdB to 80, if needed. Use colour analyser and monitor the colour temperature (X,Y) on colour analyser. Select WdR and WdB by pressing up/down buttons and change the values by Left/Right buttons till the following values are read:
X=285±10
Y=293±10 on the colour analyser.

CuR, CuG, CuB
Set the values of these items as 64 (constant).

YDFP
Enter a PAL B/G colour and black-white bar test pattern via RF. Adjust Y-Delay for PAL till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.
Min. Value: -07
Max. Value: 001
Recommended Value: -05

AGC
Apply PAL BG signal, VHF-3 Channel-12 and 60dBmV signal level. Adjust AGC (Automatic Gain Control) item by pressing Left/Right buttons till the voltage at AGC point (pin1 of the tuner) becomes 3.0 volts.
Min. Value: 000
Max. Value: 015
Recommended Value: 009

TLAN
Text language is set. Options are W-T, W-E, W, E. W-T will be selected.

APS
The option of APS (Automatic Program Searching) item are ON and OFF. In order to active APS installation procedure when TV is turned for the very first time, select ON. Inorder to start TV without APS installation procedure, select OFF.

T_T
This item is used for the Tuner selection. The options are SAM for SAMSUNG, THO for THOMSON, SIE for SIEMENS, MK2 and MK3 for PHILIPS MP2/MP3, ALP for ALPS and TEC for Tecnisat. Select THO.

T_P
This item is also used for the Tuner selection. The options are MK2, SAM, THO, TEM. MK2 for PHILIPS, SAM for SAMSUNG, THO for THOMSON and TEM for TEMIC. Select SAM.

YDFS
Enter a SECAM B/G colour and black-white bar test pattern via RF. Adjust Y-Delay SECAM till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-07

YDFN
Enter an NTSC colour and black-white bar test pattern via RF. Adjust Y-Delay NTSC till the colour transients on the colour bar of the pattern become as sharper and colours between transients do not mix with each other as possible.

Min. Value:	-07
Max. Value:	001
Recommended Value:	-02

EXT3
Select ON.

DVD
Select OFF.

C.M
Select ON.

BLUE
Select OFF.

4:3
Set to 0.

OVM
Select ON.

16.4.SERVICE ALIGNMENTS
IMPORTANT: There will no adjustments in this service mode during production mode alignments.
Press BLUE colour button on the remote control when Production mode is active. Press the colour button of the related item group headline colour. Press up/down buttons to select the item of group. Press Left/Right button to alter the value of the item. Press OK button to store the selected value and MENU button to exit the service alignments mode.

ADJUSTMENTS GROUP
Press RED button in order to access this group of items.

PIP CNTRST	: Level of the PIP picture
PIP Ydelay	: Luma delay of the PIP picture
PIP Frame	: Colour selection of the PIP frame (edges of the PIP)
EHTHP	: EHT compensation coefficient for horizontal phase
EHTH TC	: EHT time constant for horizontal phase compensation
EHTH	: EHT compensation coefficient for horizontal amplitude
EHTV	: EHT compensation coefficient for vertical amplitude
EHTV TC	: EHT time constant for control of vertical and horizontal amplitude EHT compensation
SVDEL	: Delay adjustment for scan velocity modulation
BCLTHR (mA)	: Beam current applied to the CRT
OSD CONT	: Contrast level of OSD
OSD BRI	: Brightness level of OSD
TEXT BRI	: Brightness level of text
PIP YDelSe	: Y-Delay adjustment for pin-in-picture option
INIT NVM	: Press to initiate the NVM

PRESCALER GROUP

Press GREEN button in order to access this group of items.

FM	: This adjustment is to determine the pre-amplifier gain of MSP for German stereo Set to 27.
NICAM	: This adjustment is to determine the pre-amplifier gain of MSP for Nicam Set to 61.
I2S	: Not used.
SCART	: This adjustment is to determine the pre-amplifier gain of MSP for Scart audio inputs Set to 25.

OPTIONS GROUP

Press BLUE button in order to access this group of items.

0.HPHONE	: ON/OFF
1.CRT	: 4:3 / 16:9
2.SVHS	: ON/OFF
3.f(IF)	: always set to 38.9
4.Türk.	: Turkish menu ON/OFF
5.VGA	: ON/OFF
6.FRONT	: Front AV ON/OFF
7.DPL	: ON/OFF
8.VD	: ON/OFF
9.NSL	: ON/OFF
A.PAP	: ON/OFF
B.CTI	: ON/OFF
C.AVL	: ON/OFF

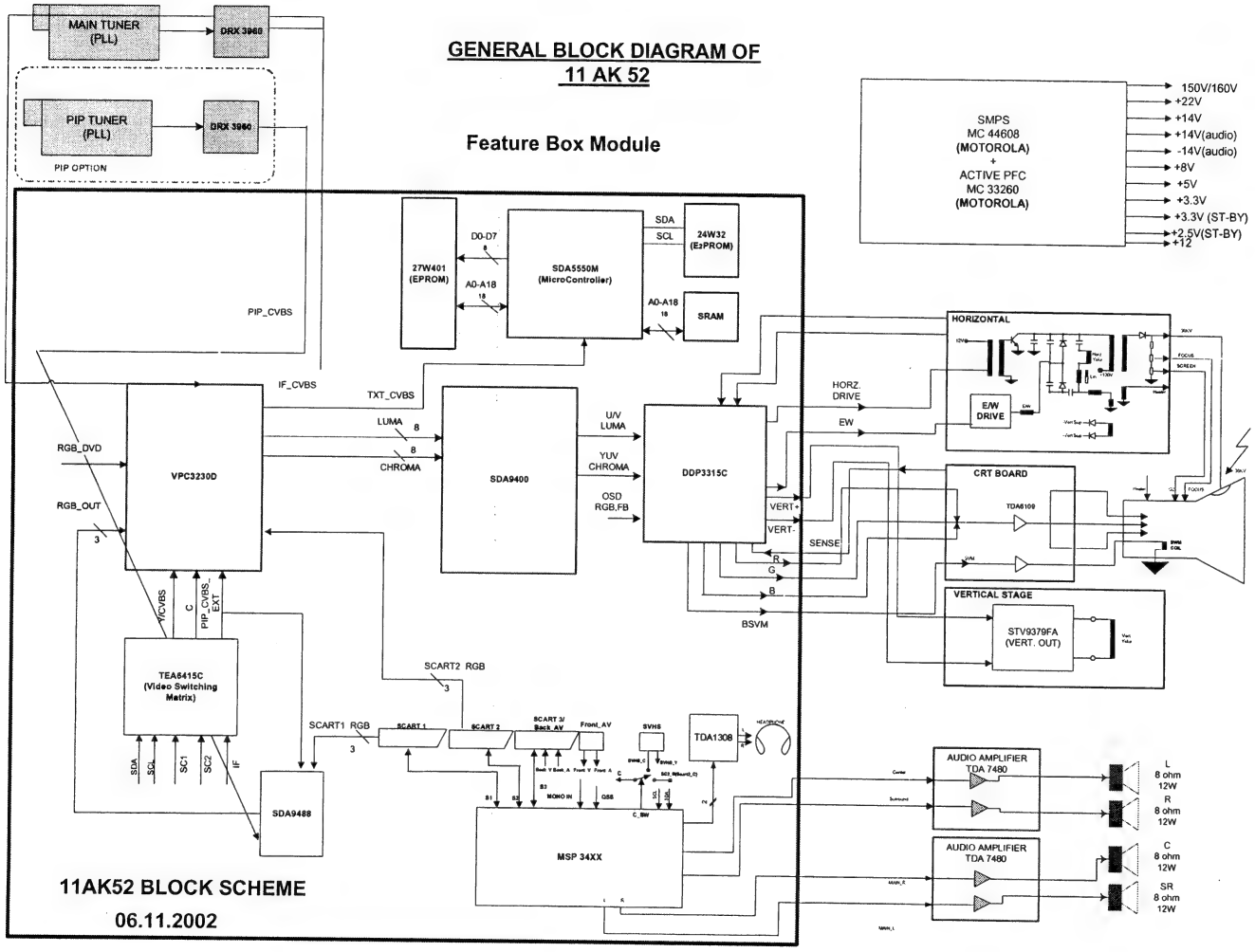
SYSTEM GROUP

Press YELLOW button in order to access this group of items.

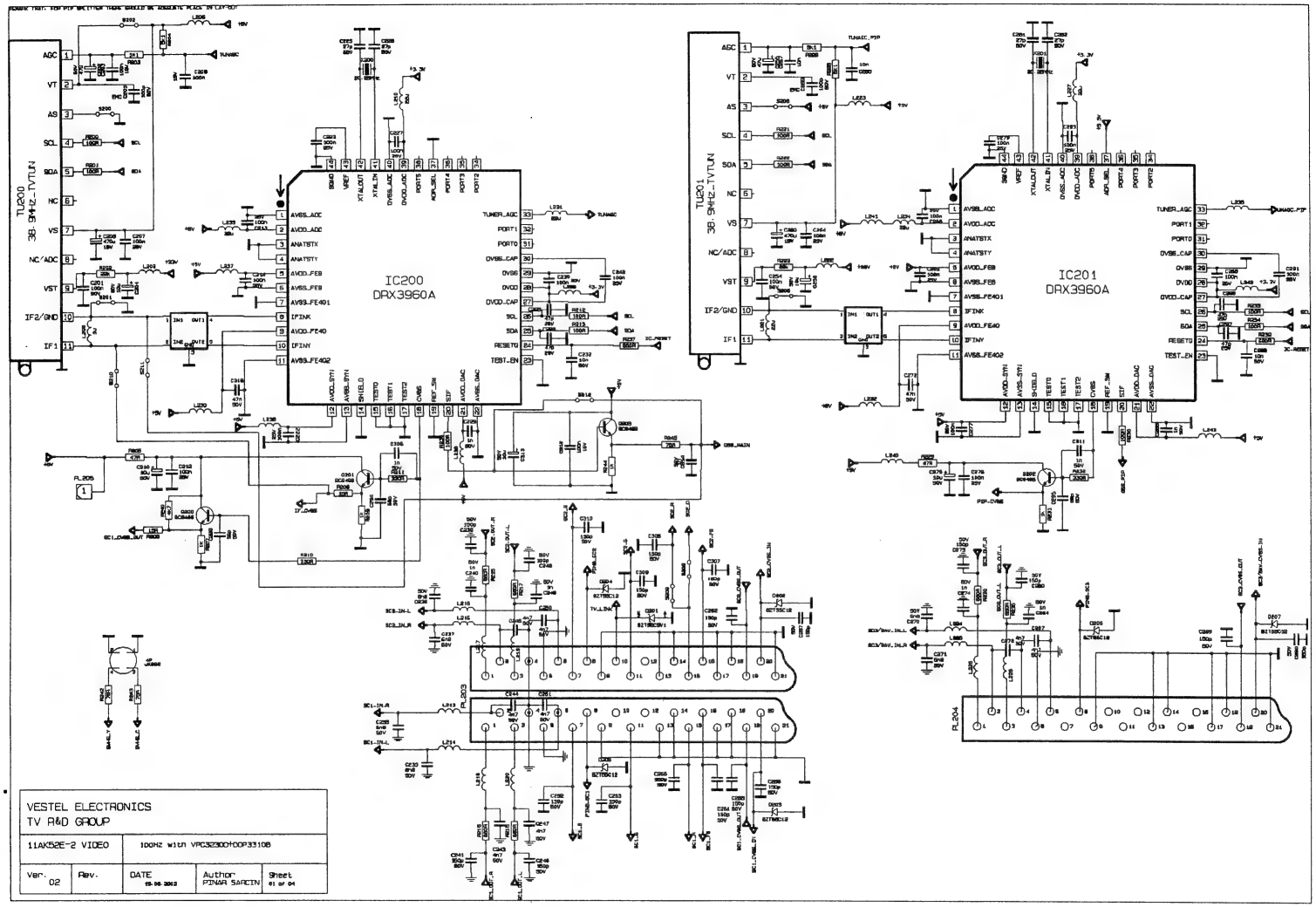
0.PAL B/G	: ON/OFF
1.PAL D/K	: ON/OFF
2.PAL I	: ON/OFF
3.SECAM B/G	: ON/OFF
4.SECAM D/K	: ON/OFF
5.SECAM L/L'	: ON/OFF
6.AUST.	: ON/OFF

NOTE: Settings values in Service menu are given for 28" 4:3 THOMSON (A66EHJ13X12) tube in this manual.

17.BLOCK DIAGRAM



18.CIRCUIT DIAGRAMS



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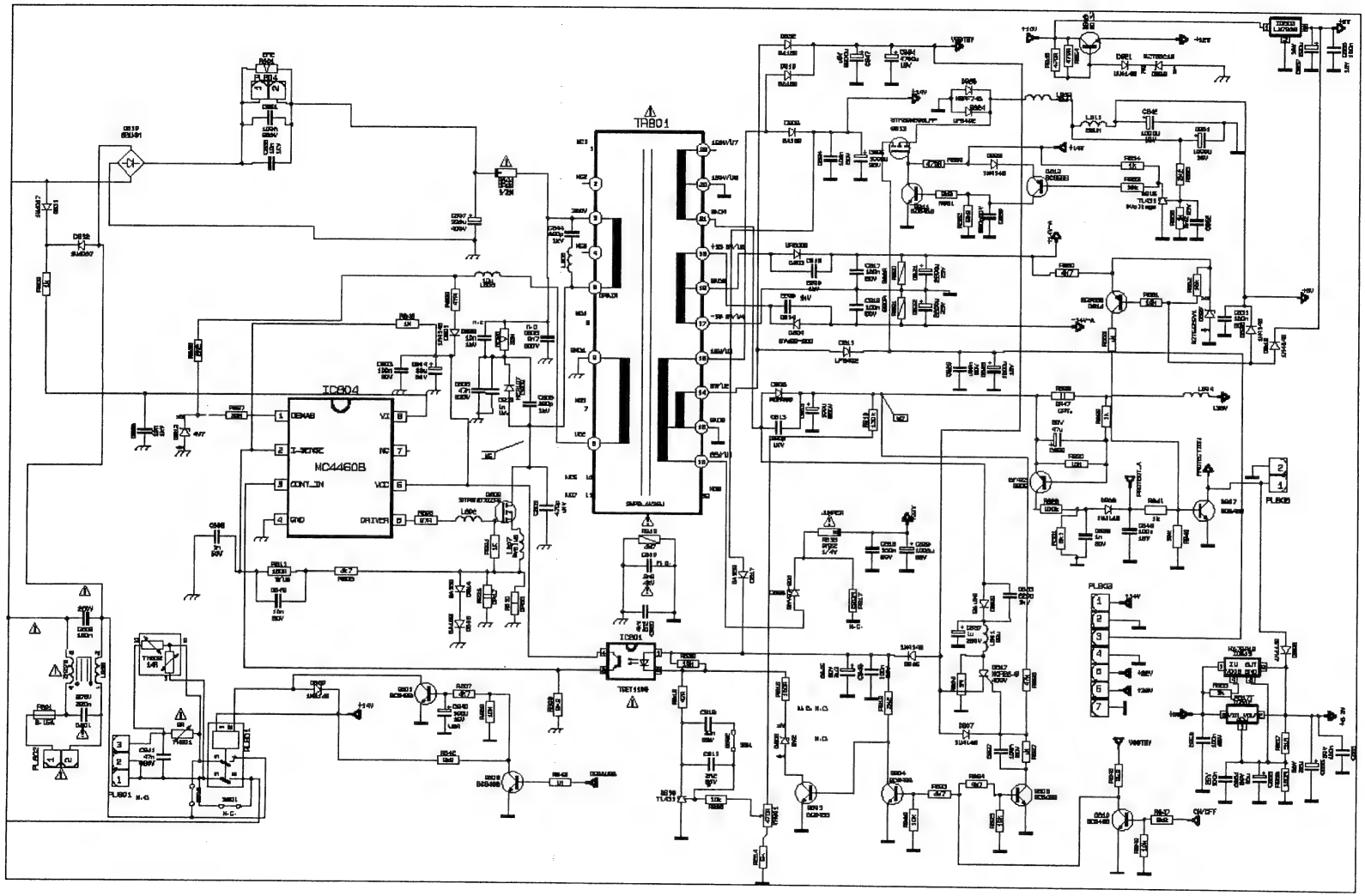

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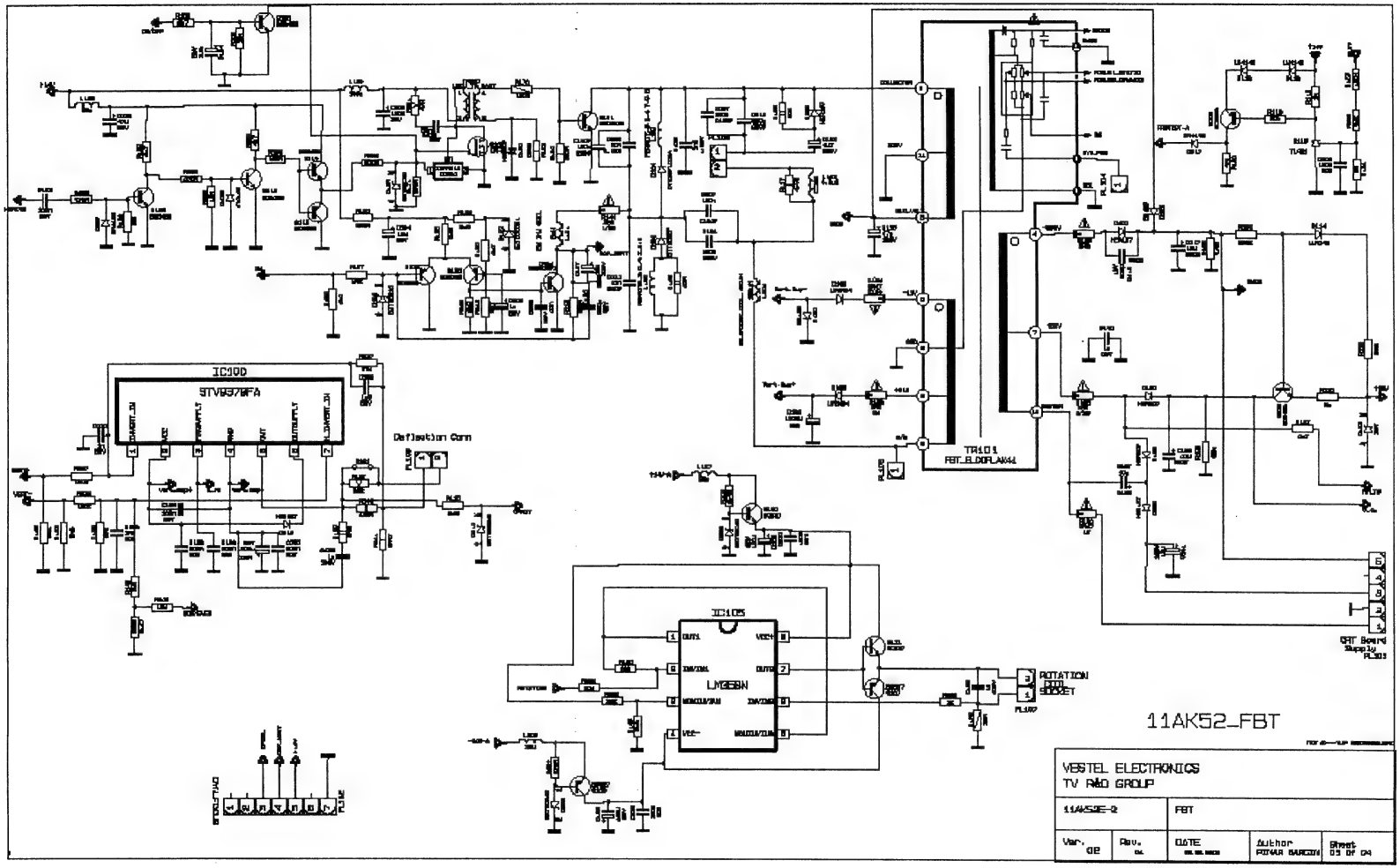
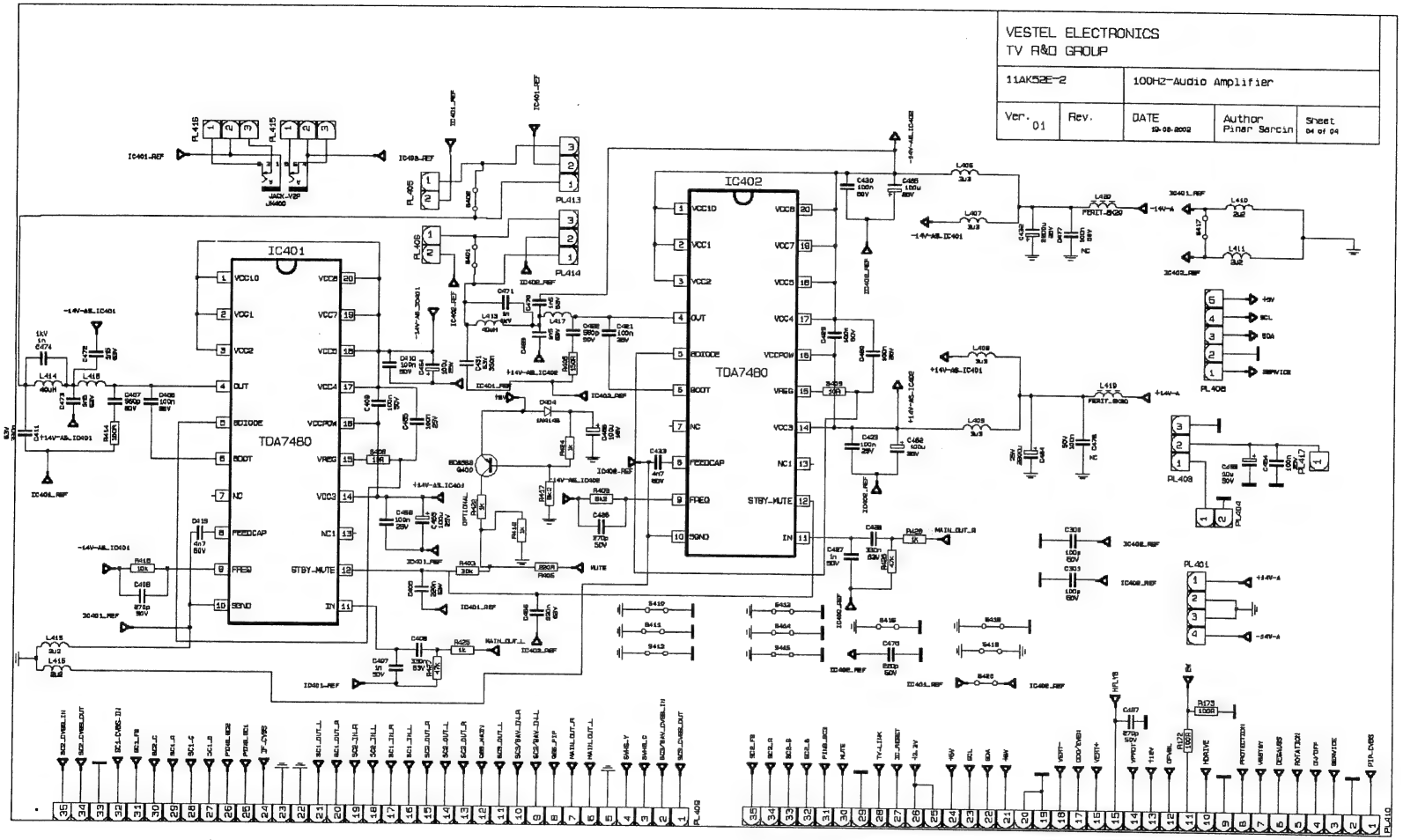
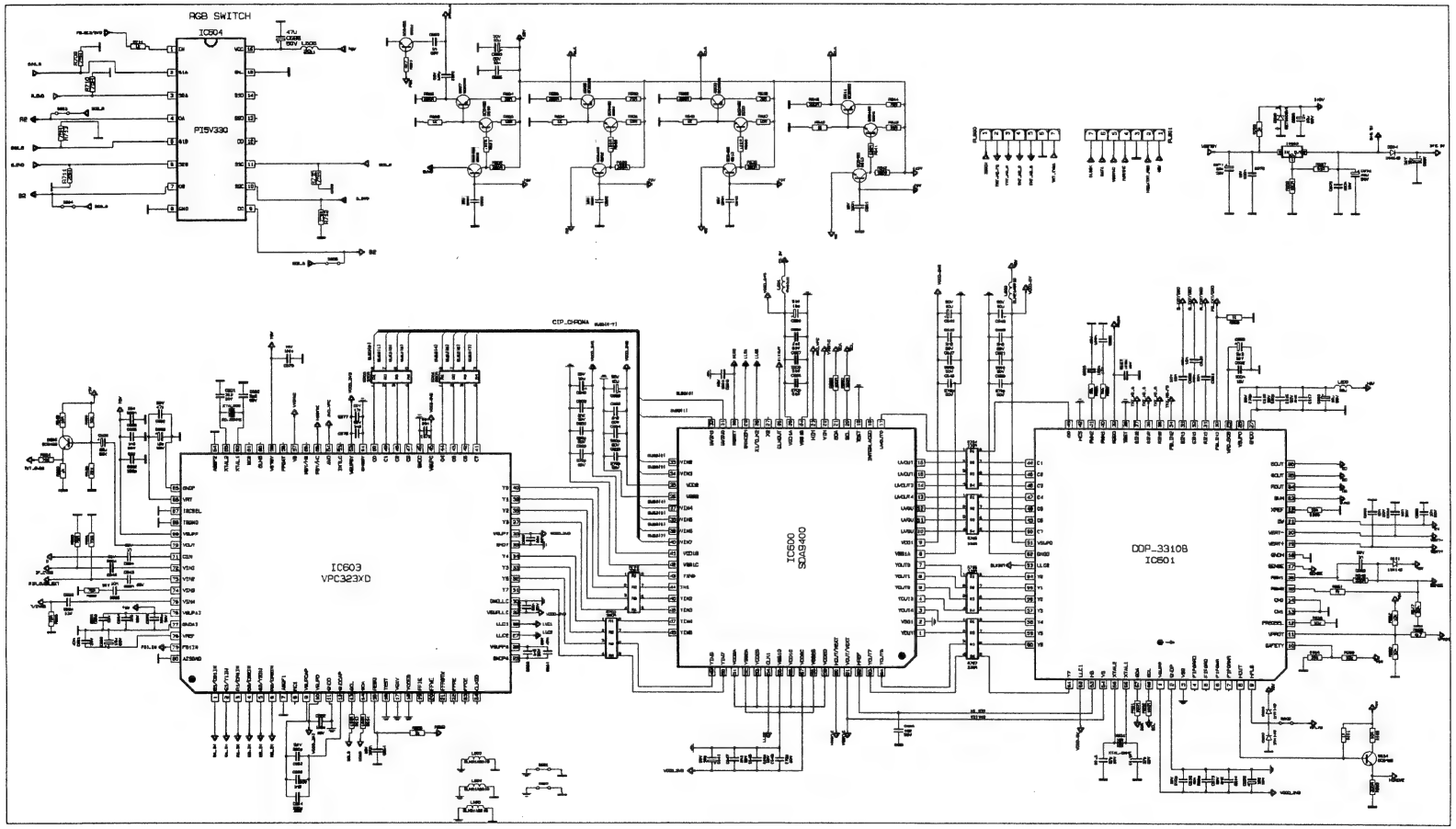

IC10D
STV9379FA
Deflection Conn
IC1105
LM1881N
TR101
FBT_BLOCPLAN44
ROTATION
COIL
SOCKET
11AK52_FBT
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
FBT

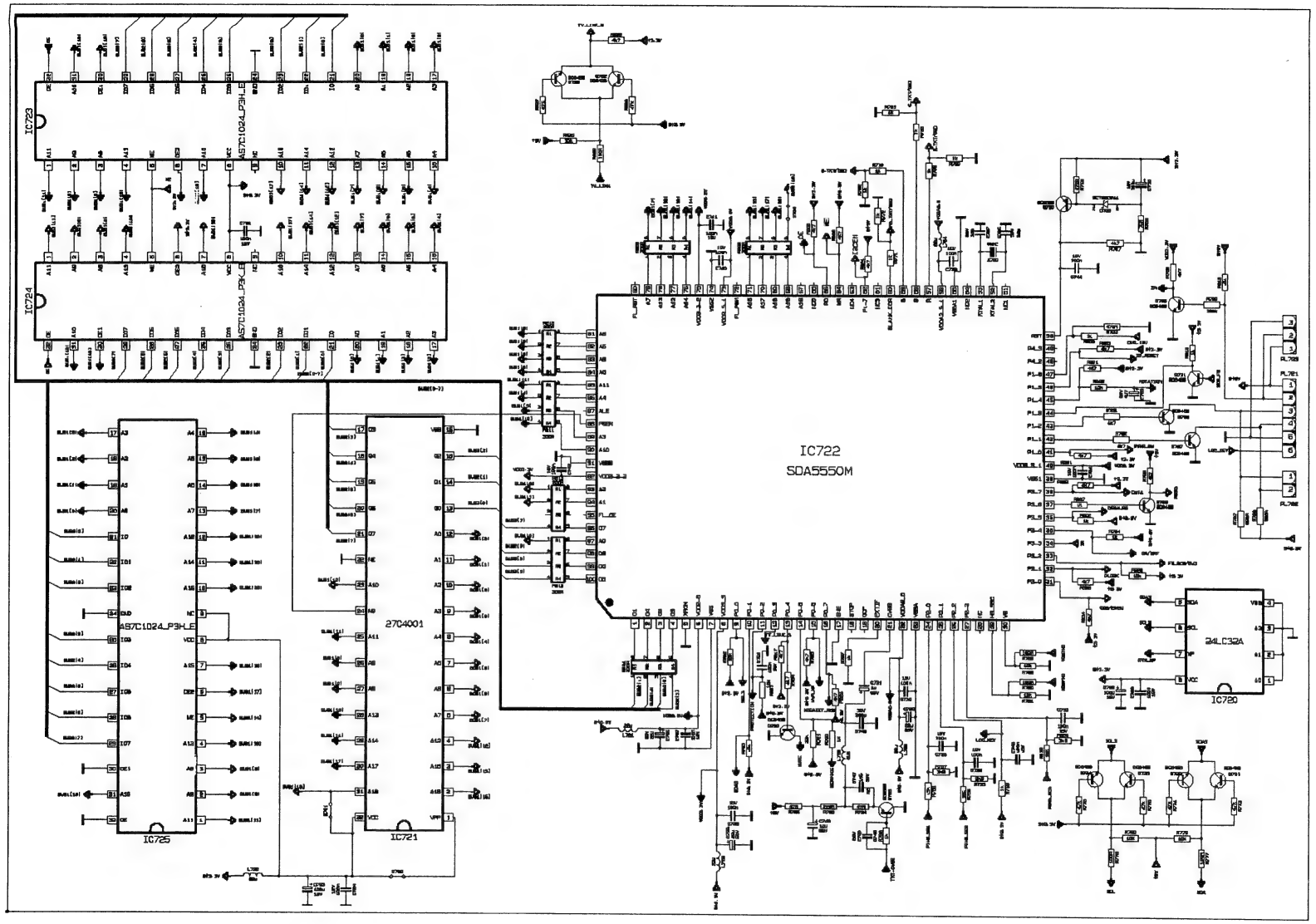
11ak52e3-3


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
100HZ-Audio Amplifier
Ver. 01
Rev.
DATE 12-08-2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480

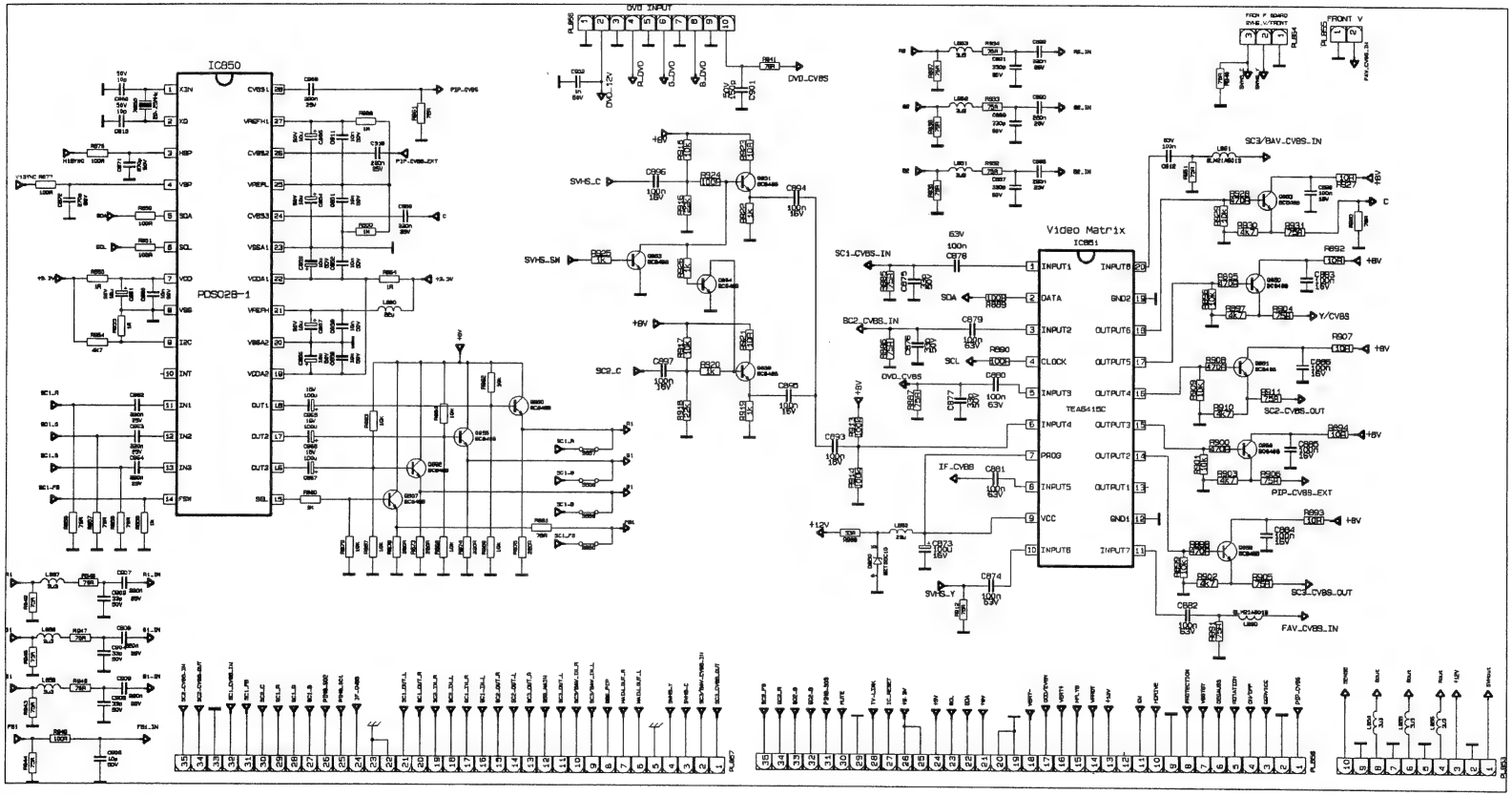
11ak52e3-4


RGB SWITCH
IC604
PI5V330
IC603
VPC323XD
IC600
SDA9400
DDP_3310B
IC601

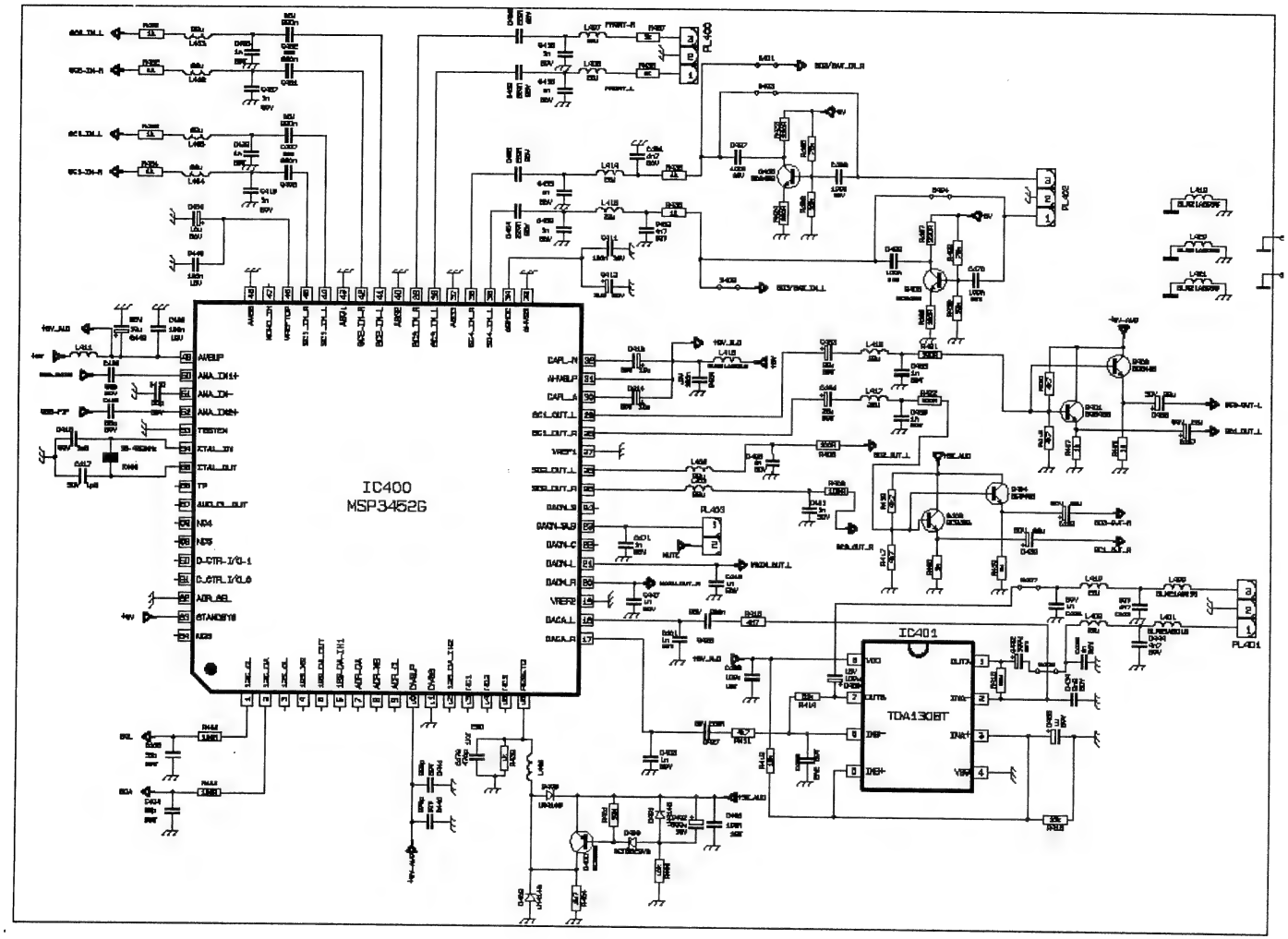
11fb2a1—1


IC722
SDA5550M
IC723
IC724
IC725
IC721
IC720
AS7C1024_P3H_E
2704001
24LC32A

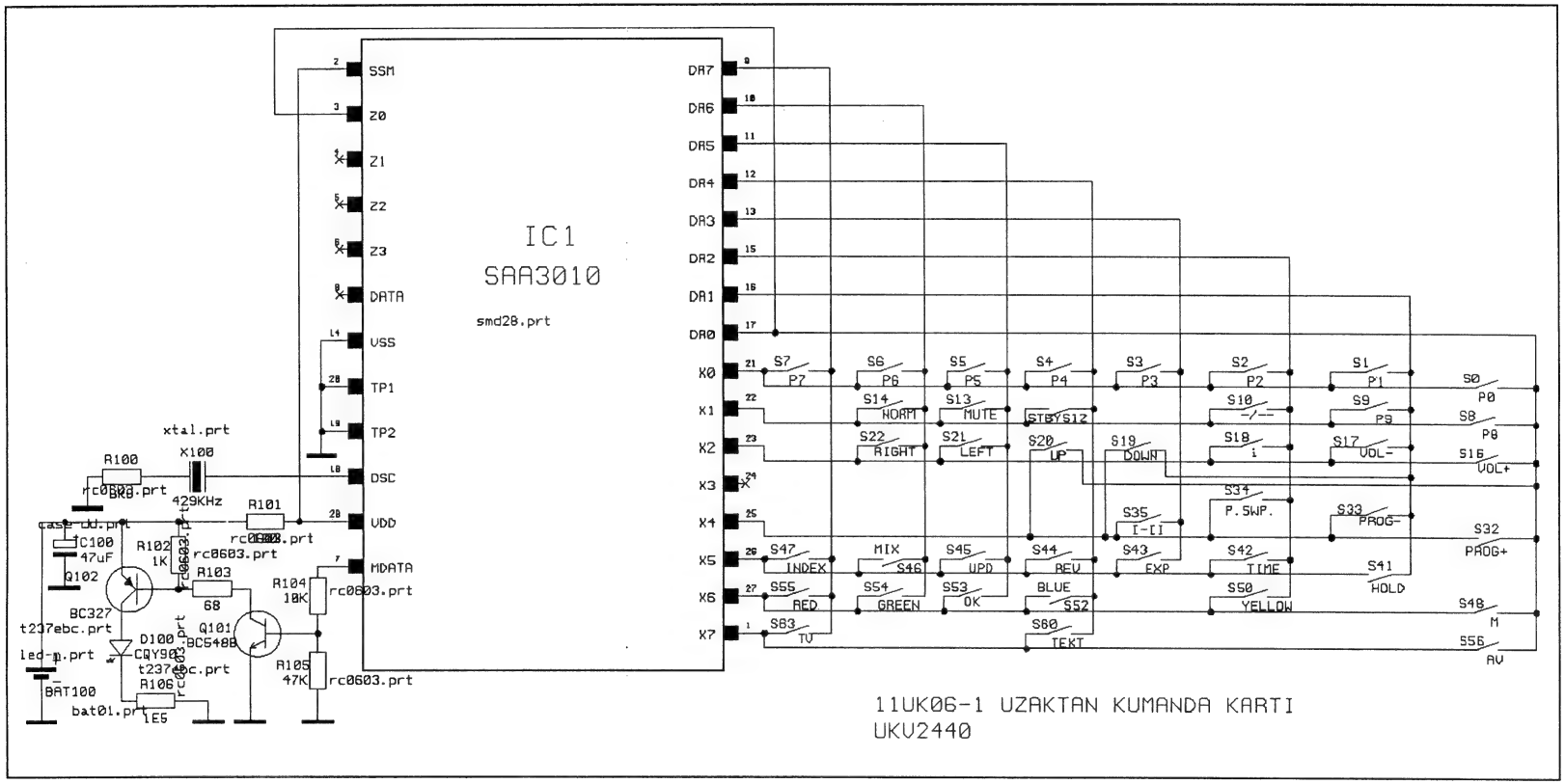
11fb2a1—2


IC850
PDS02B-1
DVB INPUT
DVD_CVBS
P3P_CVBS
P3P_CVBS_EXT
SVHS_C
SVHS_SM
SC2_C
Video Matrix
IC851
TEA5415C
SC1_CVBS_IN
BC2_CVBS_IN
DVD_CVBS
IF_CVBS
SVHS_Y
SC3/BAV_CVBS_IN
Y/CVBS
SC2_CVBS_OUT
PIP_CVBS_EXT
SC3_CVBS_OUT
FAV_CVBS_IN
FRONT V

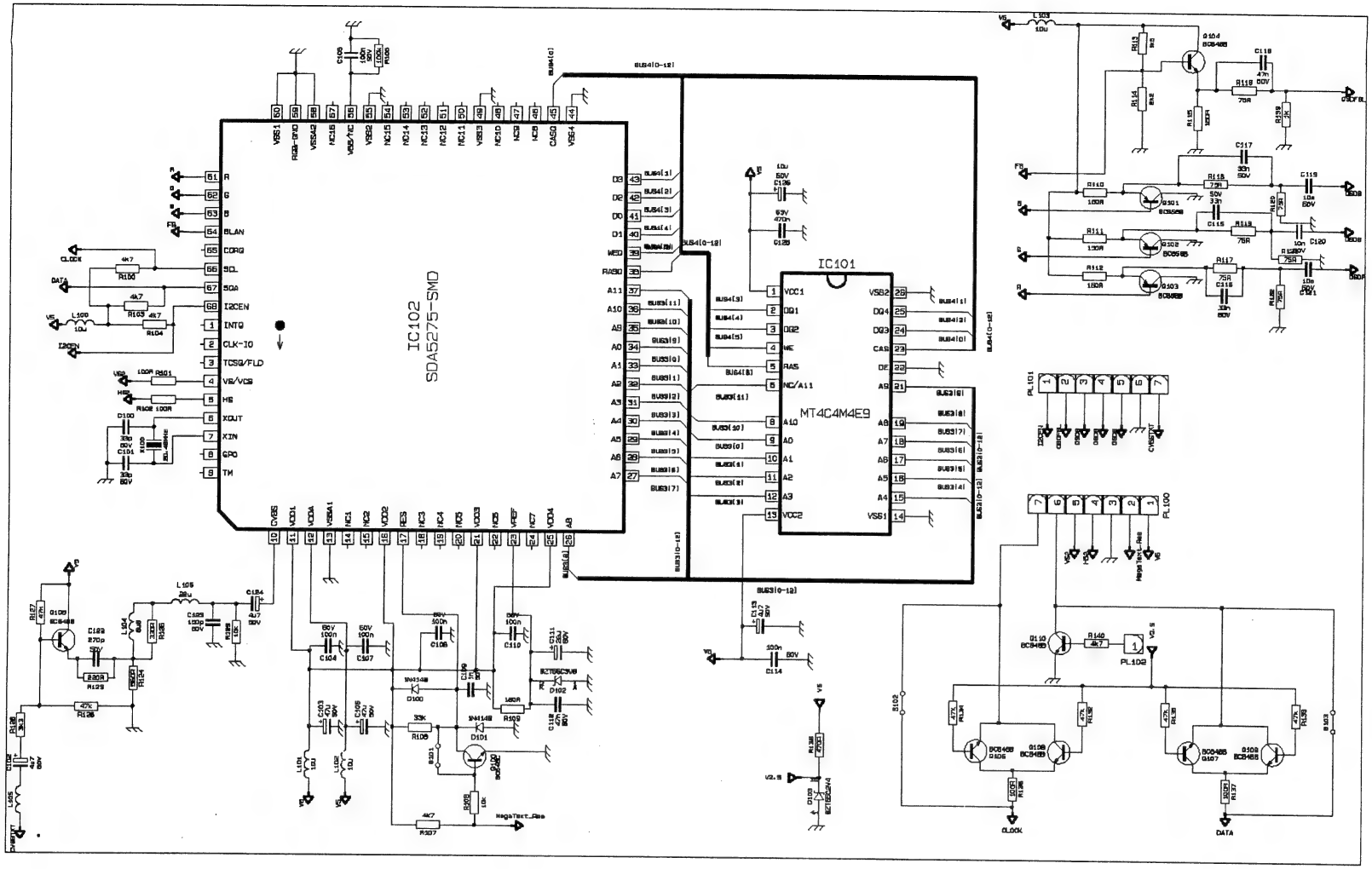
11fb2a1—3



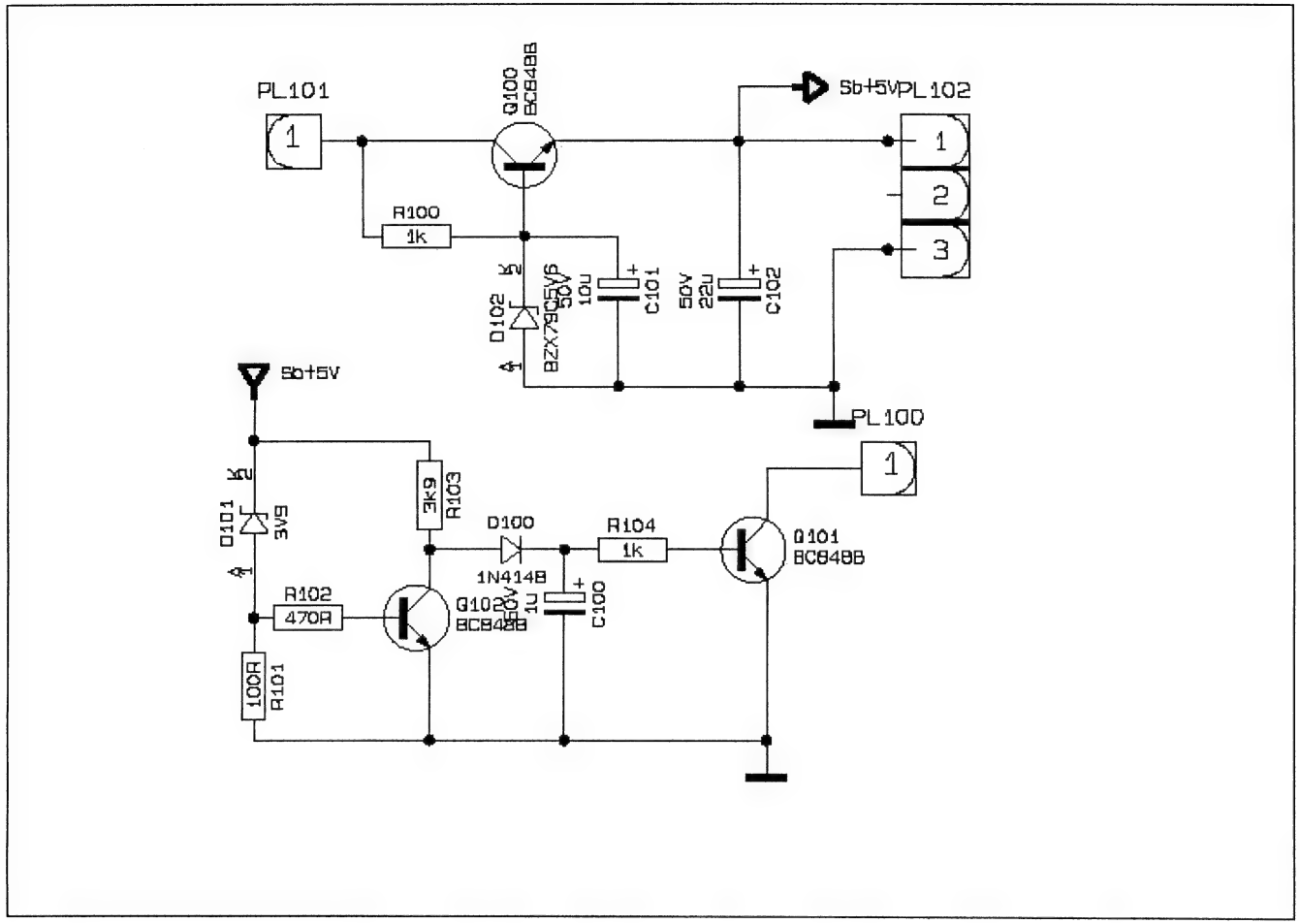
11fb2a1—4


IC1
SAA3010
smd28.prt
SSM
Z0
Z1
Z2
Z3
DATA
VSS
TP1
TP2
OSC
VDD
MDATA
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
K0
K1
K2
K3
K4
K5
K6
K7
xtal.prt
X100
429KHz
R100
R101
R102
1K
R103
68
R104
10K
R105
47K
R106
1E5
C100
47uF
Q102
BC327
Q101
BC548B
D100
CQY90
BAT100
bat01.prt
led-1.prt
S7 P7
S6 P6
S5 P5
S4 P4
S3 P3
S2 P2
S1 P1
S0 P0
S14 NORM
S13 MUTE
S12
S10 -/--
S9 P9
S8 P8
S22 RIGHT
S21 LEFT
S20 UP
S19 DOWN
S18 i
S17 VOL-
S16 VOL+
S34 P.SWP.
S35 I-[]
S33 PROG-
S32 PROG+
S47 INDEX
S46 MIX
S45 UPD
S44 REV
S43 EXP
S42 TIME
S41 HOLD
S55 RED
S54 GREEN
S53 OK
S52 BLUE
S50 YELLOW
S48 M
S56 AV
S83 TV
S80 TEXT
11UK06-1 UZAKTAN KUMANDA KARTI
UKU2440

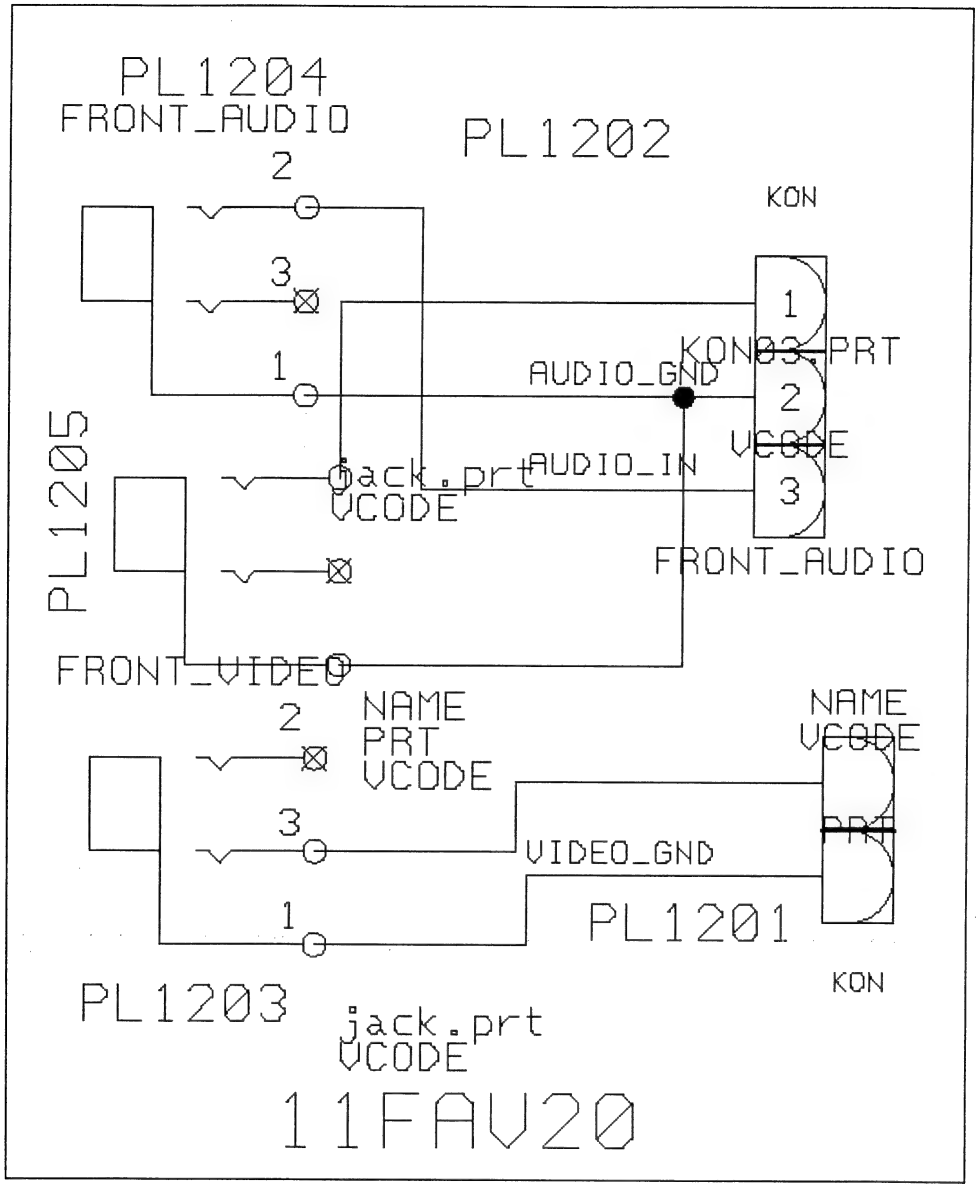
11uk06-1



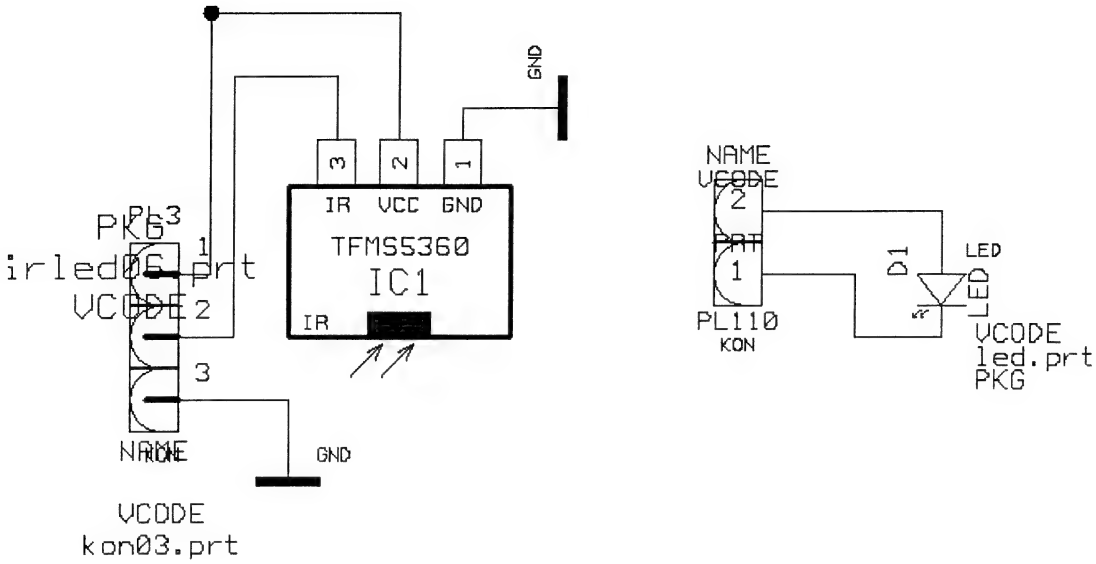
11txt52-3


PL101
1
Q100
BC848B
Sb+5V
PL102
1
2
3
R100
1k
D102
BZX79C5V6
50V
10u
C101
50V
22u
C102
Sb+5V
PL100
1
D101
3V9
3k9
R103
D100
1N4148
R104
1k
Q101
BC848B
R102
470R
Q102
BC848B
50V
1u
C100
100R
R101

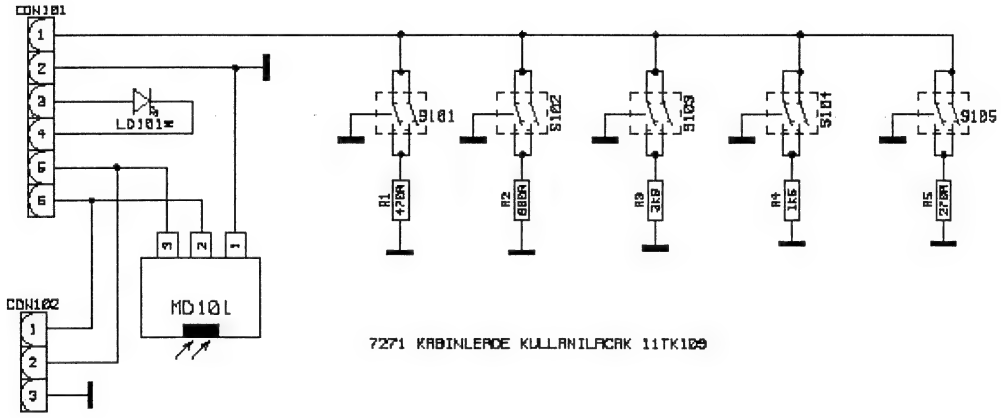
11rs52


PL1204
FRONT_AUDIO
2
3
1
PL1205
jack.prt
VCODE
FRONT_VIDEO
PL1202
KON
1
2
3
AUDIO_GND
AUDIO_IN
FRONT_AUDIO
2
NAME
PRT
VCODE
3
1
PL1203
jack.prt
VCODE
NAME
VCODE
VIDEO_GND
PL1201
KON
11FAV20

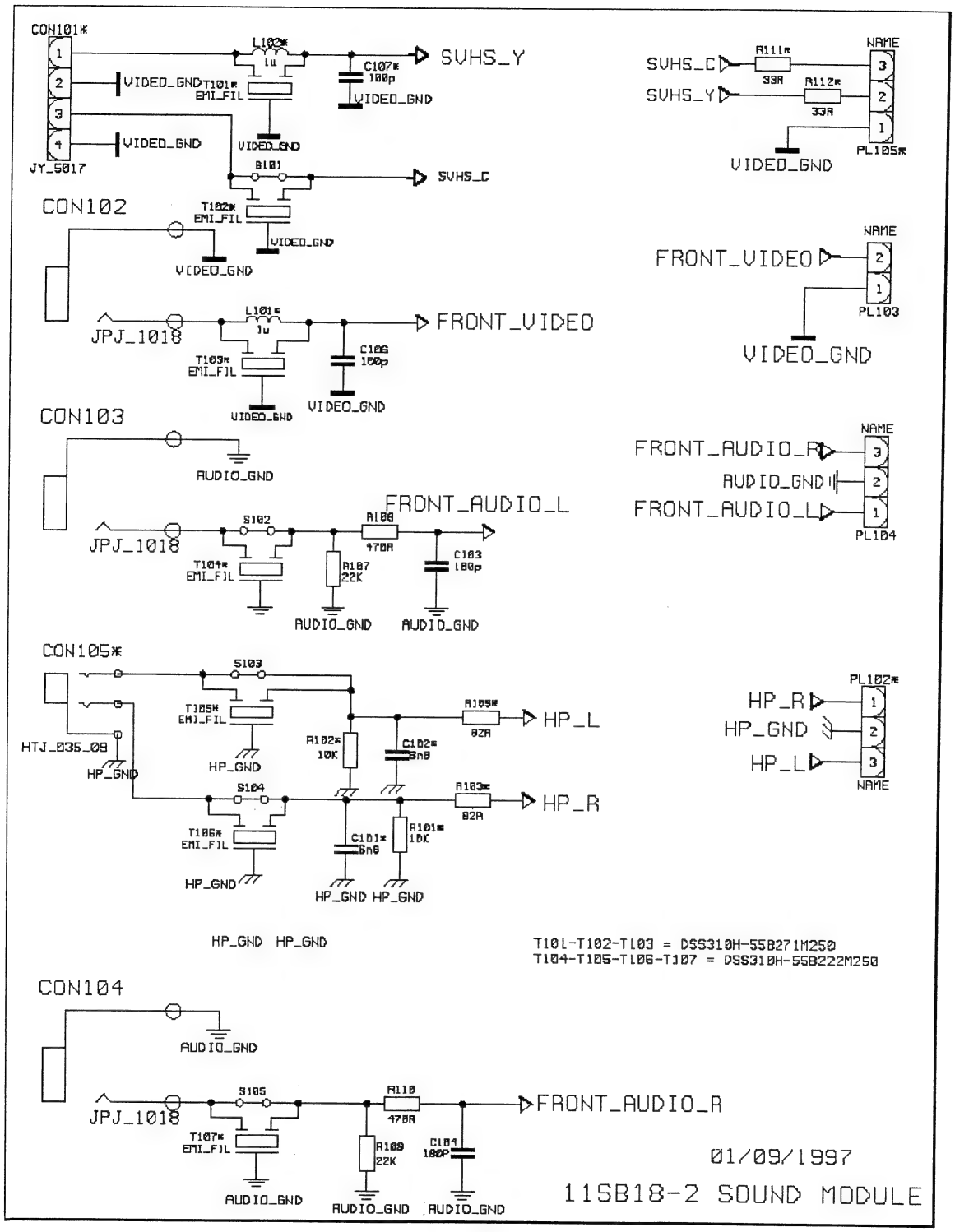
11fav19a4



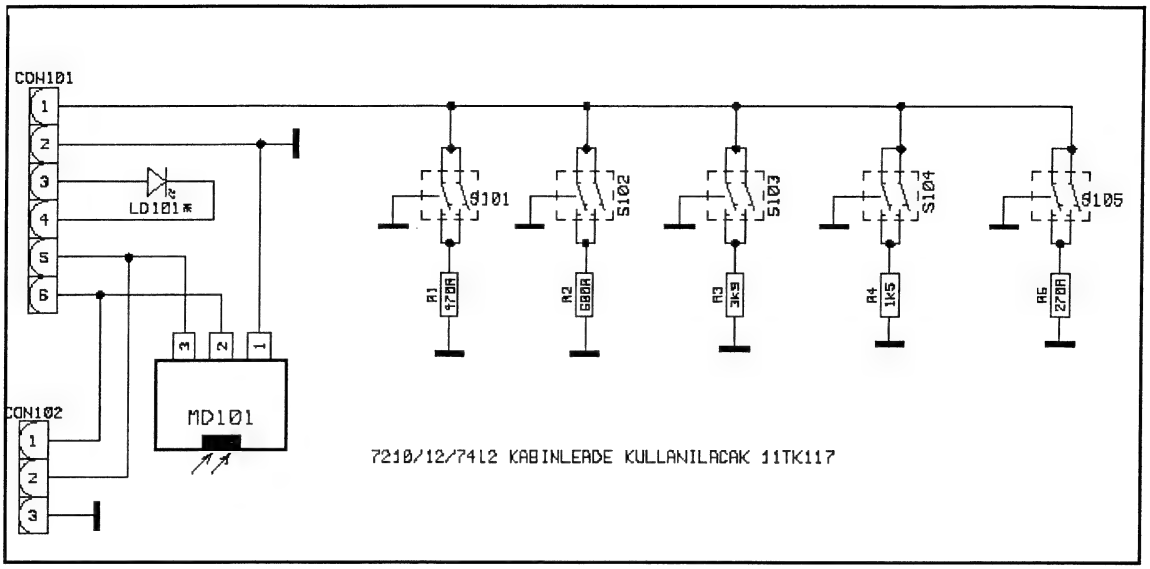
11ir2872



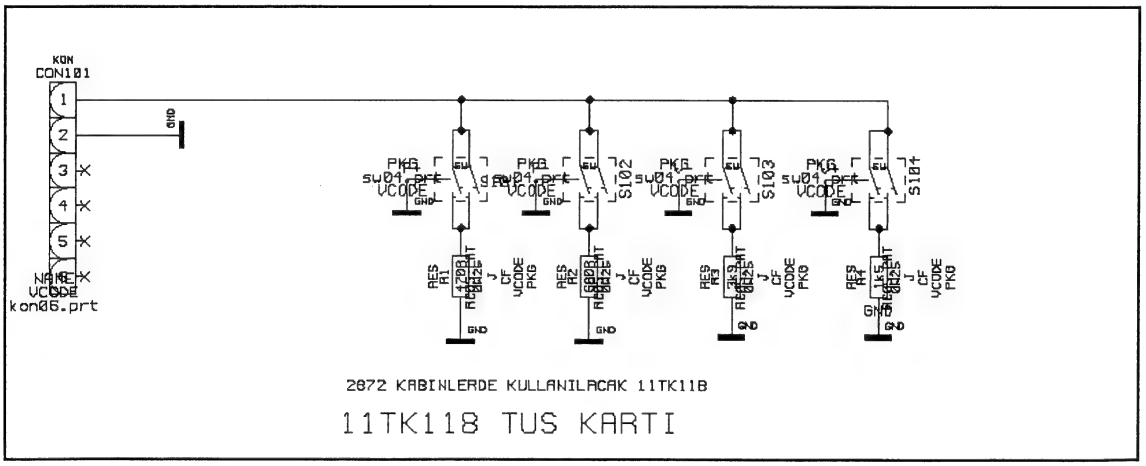
11tk109


CON101*
JY_5017
L102*
1u
C107*
100p
SVHS_Y
VIDEO_GND
T101*
EMI_FIL
G101
SVHS_C
CON102
T102*
EMI_FIL
JPJ_1018
L101*
1u
FRONT_VIDEO
T103*
EMI_FIL
C106
100p
CON103
AUDIO_GND
FRONT_AUDIO_L
S102
R108
470R
T104*
EMI_FIL
R107
22K
C103
100p
CON105*
S103
T105*
EMI_FIL
R105*
0ZR
HP_L
HTJ_035_09
HP_GND
R102*
10K
C102*
3n9
S104
R103*
0ZR
HP_R
T106*
EMI_FIL
C101*
6n8
R101*
10K
CON104
S105
R110
470R
T107*
EMI_FIL
R109
22K
C104
100P
FRONT_AUDIO_R
SVHS_C
SVHS_Y
R111*
33R
R112*
33R
NAME
PL105*
FRONT_VIDEO
PL103
FRONT_AUDIO_R
AUDIO_GND
FRONT_AUDIO_L
PL104
HP_R
HP_GND
HP_L
PL102*
T101-T102-T103 = DSS310H-55B271M250
T104-T105-T106-T107 = DSS310H-55B222M250
01/09/1997
11SB18-2 SOUND MODULE

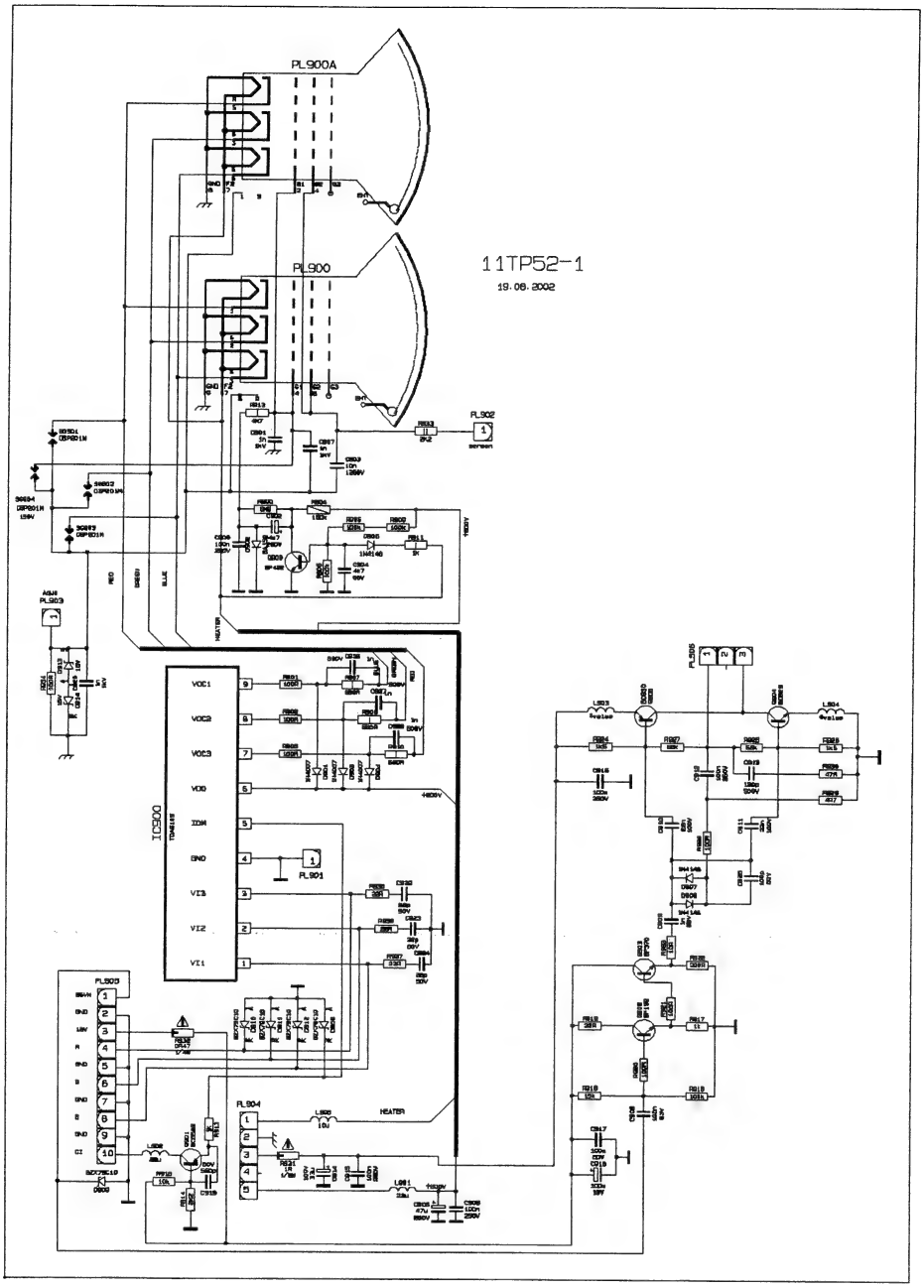
11sb18-3



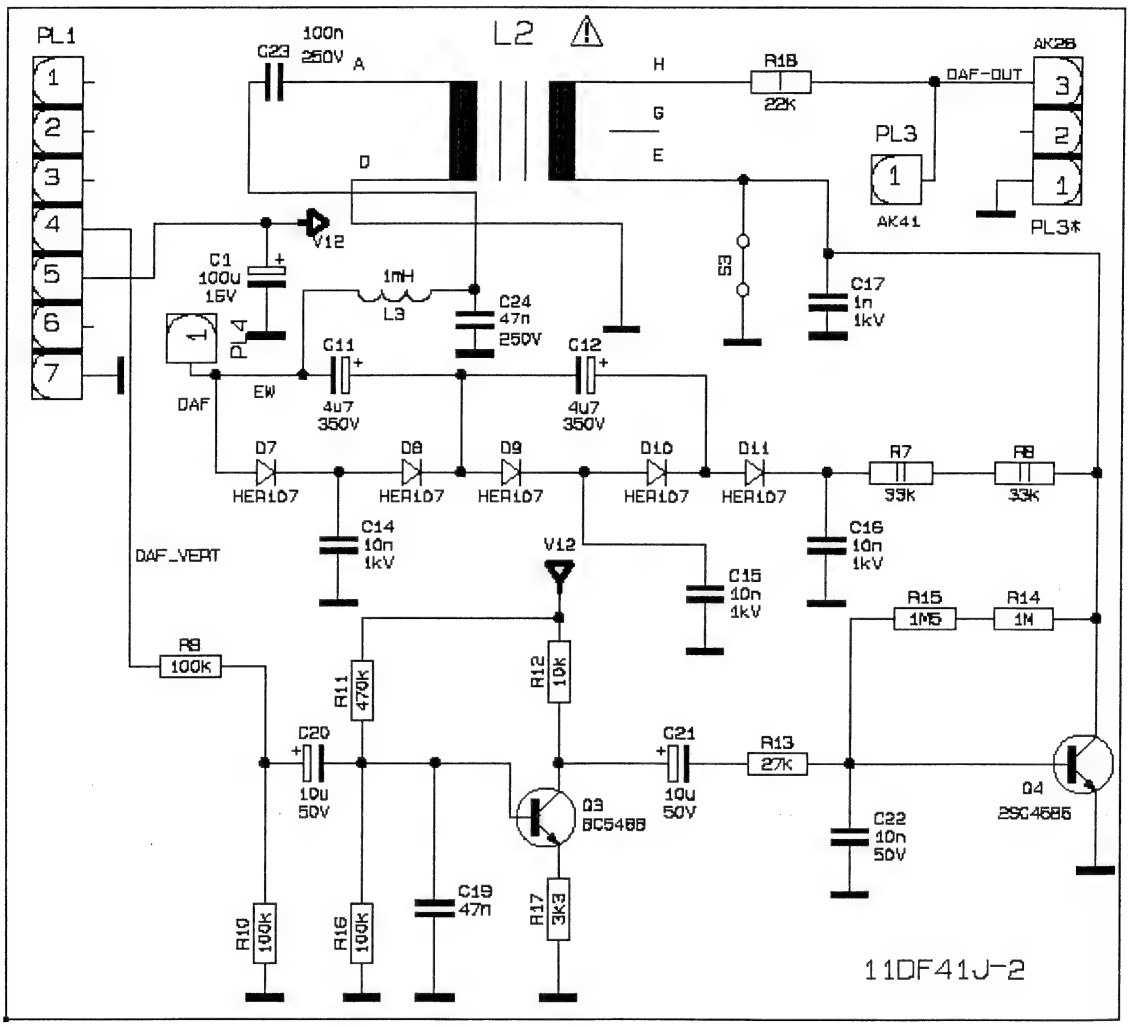
11tk117



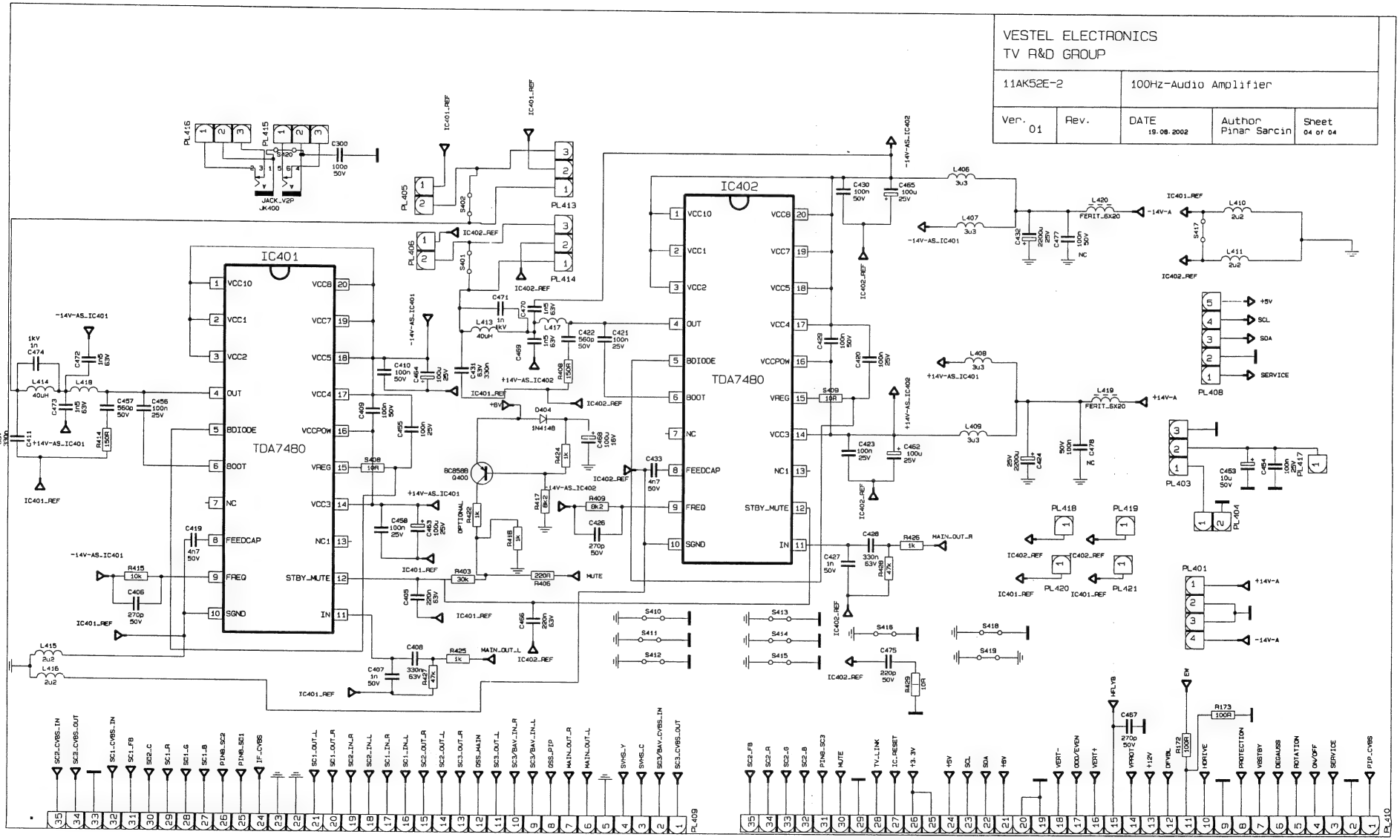
11tk118

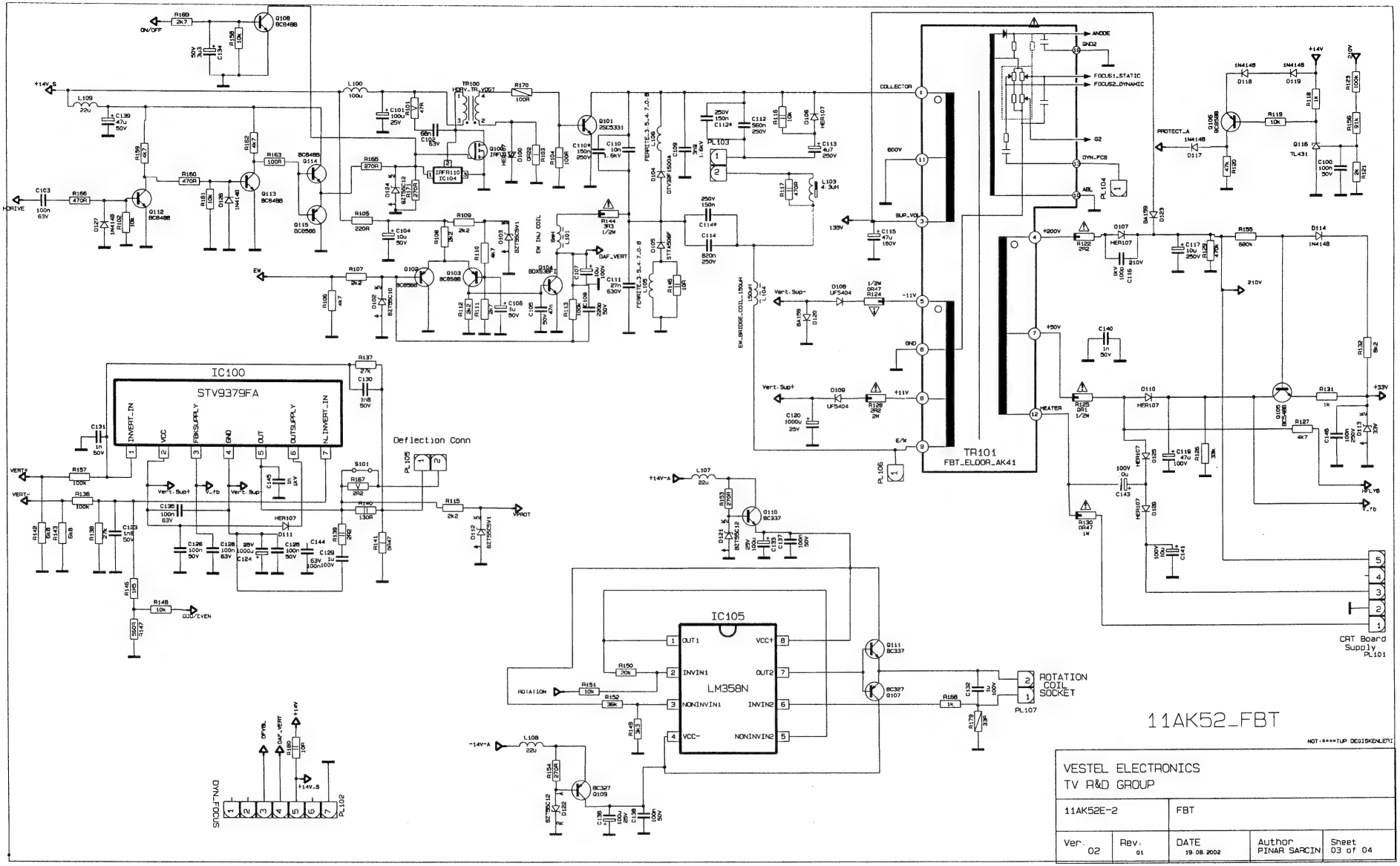

PL900A
PL900
11TP52-1
19.06.2002
PL902
PL903
PL901
PL904
PL905
IC900
HEATER

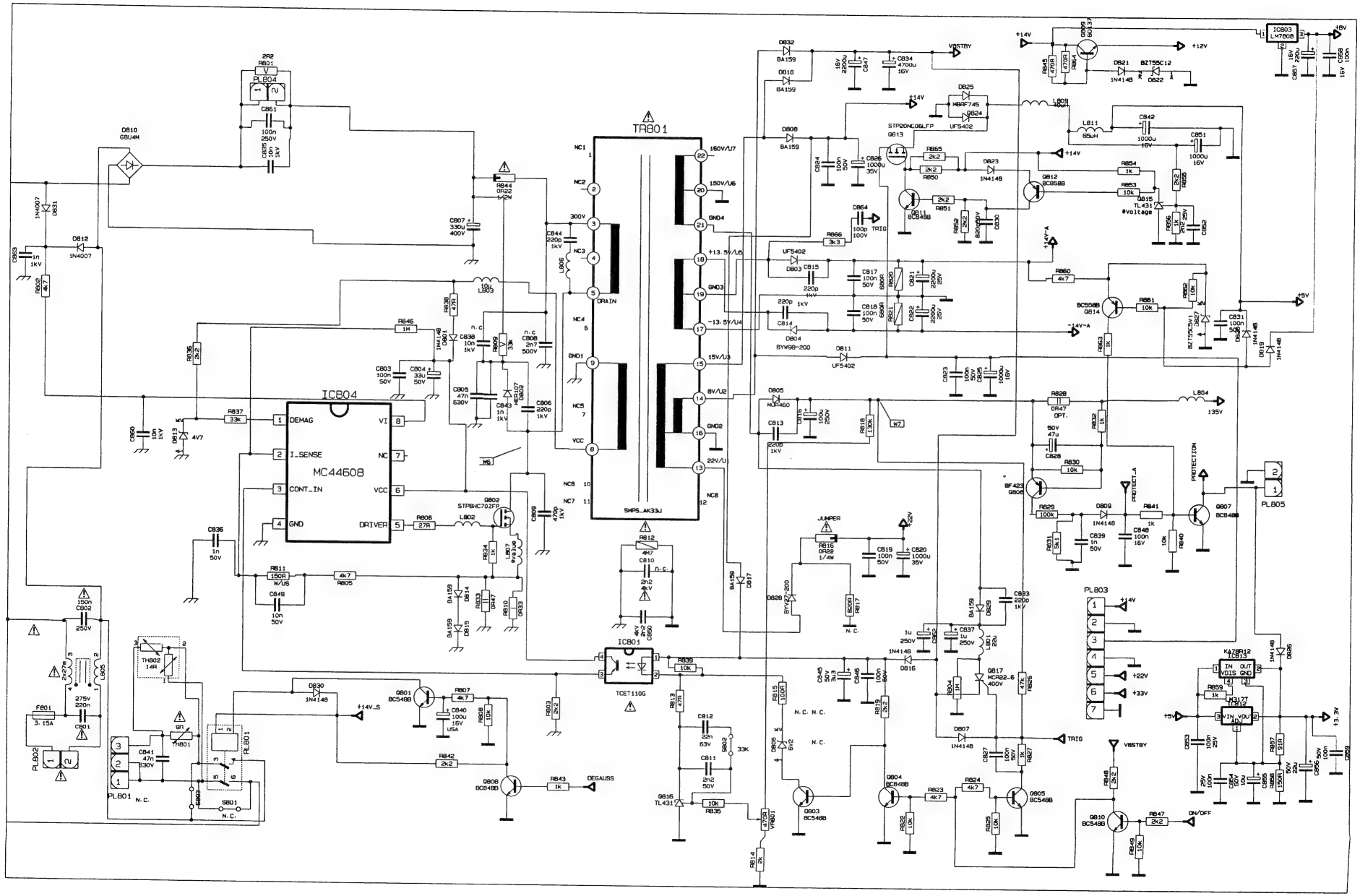
11tp52-1

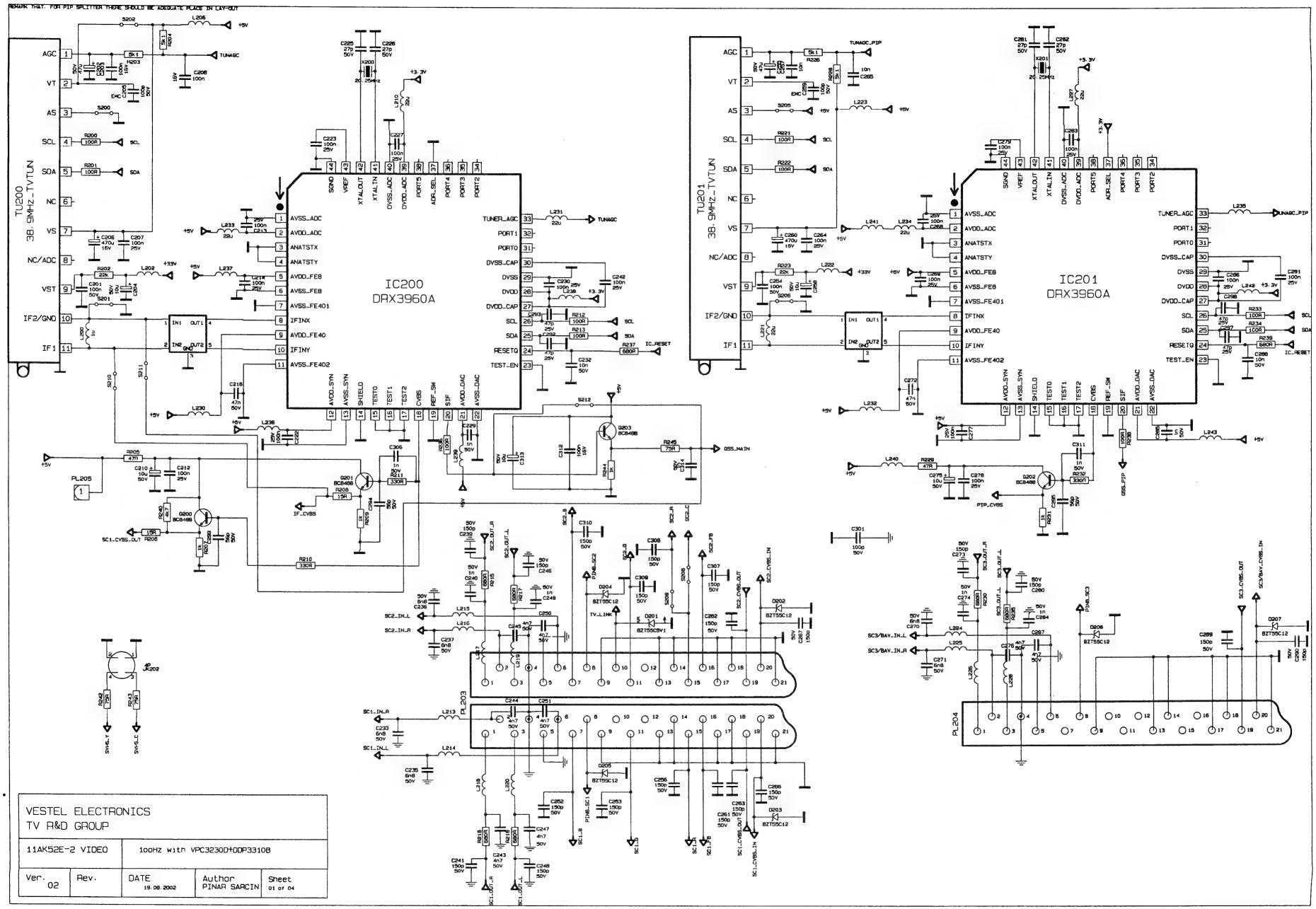

PL1
1
2
3
4
5
6
7
C23
100n
250V
A
L2
H
G
E
D
R18
22K
DAF-OUT
AK25
3
2
1
PL3
1
AK41
PL3*
V12
C1
100u
16V
1mH
L3
C24
47n
250V
S3
C17
1n
1kV
PL4
1
DAF
EW
C11
4u7
350V
C12
4u7
350V
D7
HER107
D8
HER107
D9
HER107
D10
HER107
D11
HER107
R7
33k
R8
33k
C14
10n
1kV
C16
10n
1kV
V12
C15
10n
1kV
DAF_VERT
R15
1M5
R14
1M
R9
100k
R11
470k
R12
10k
C20
10u
50V
C21
10u
50V
R13
27K
Q3
BC548B
Q4
2SC4686
C22
10n
50V
R10
100k
R16
100k
C19
47n
R17
3k3
11DF41J-2

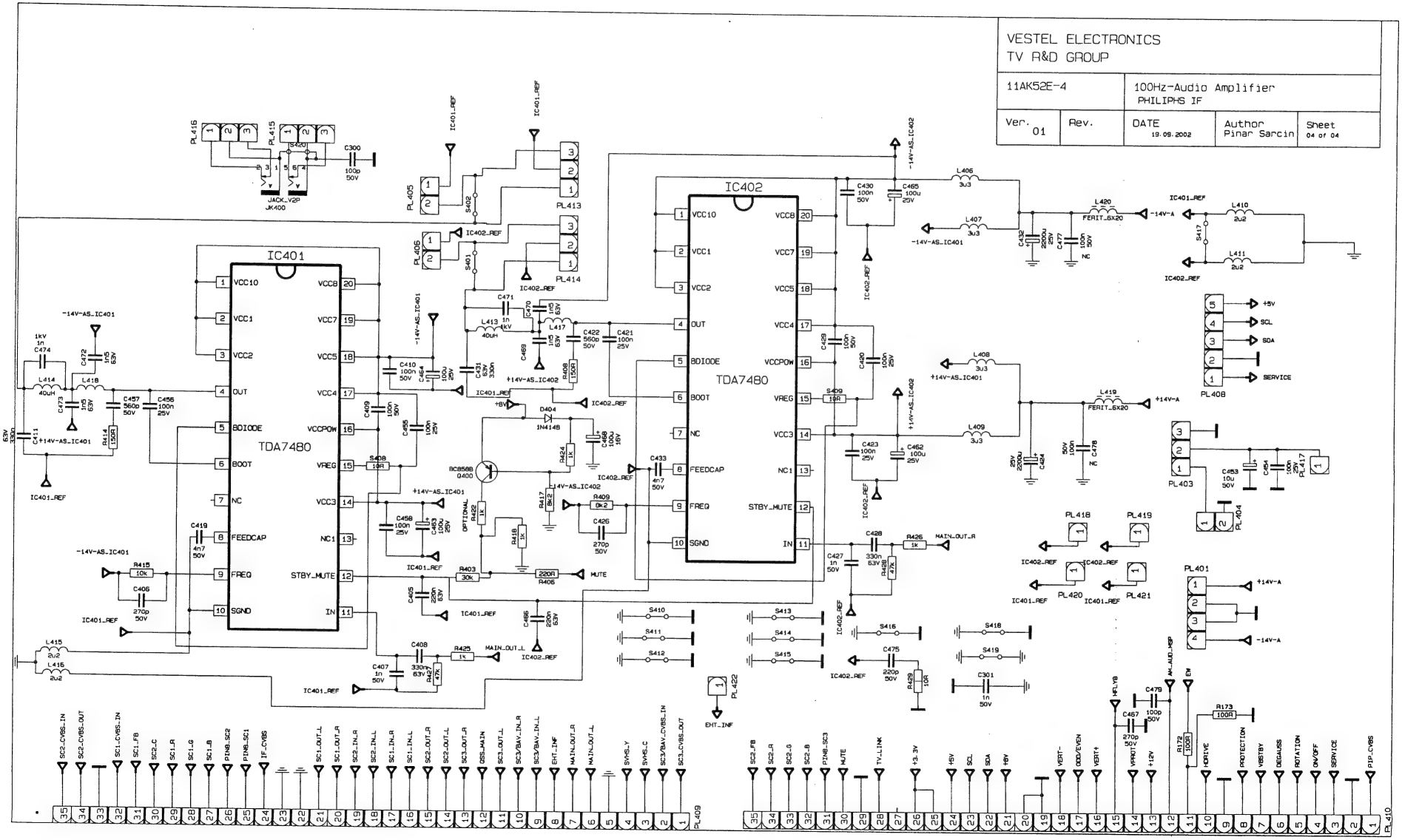
11df41j-2

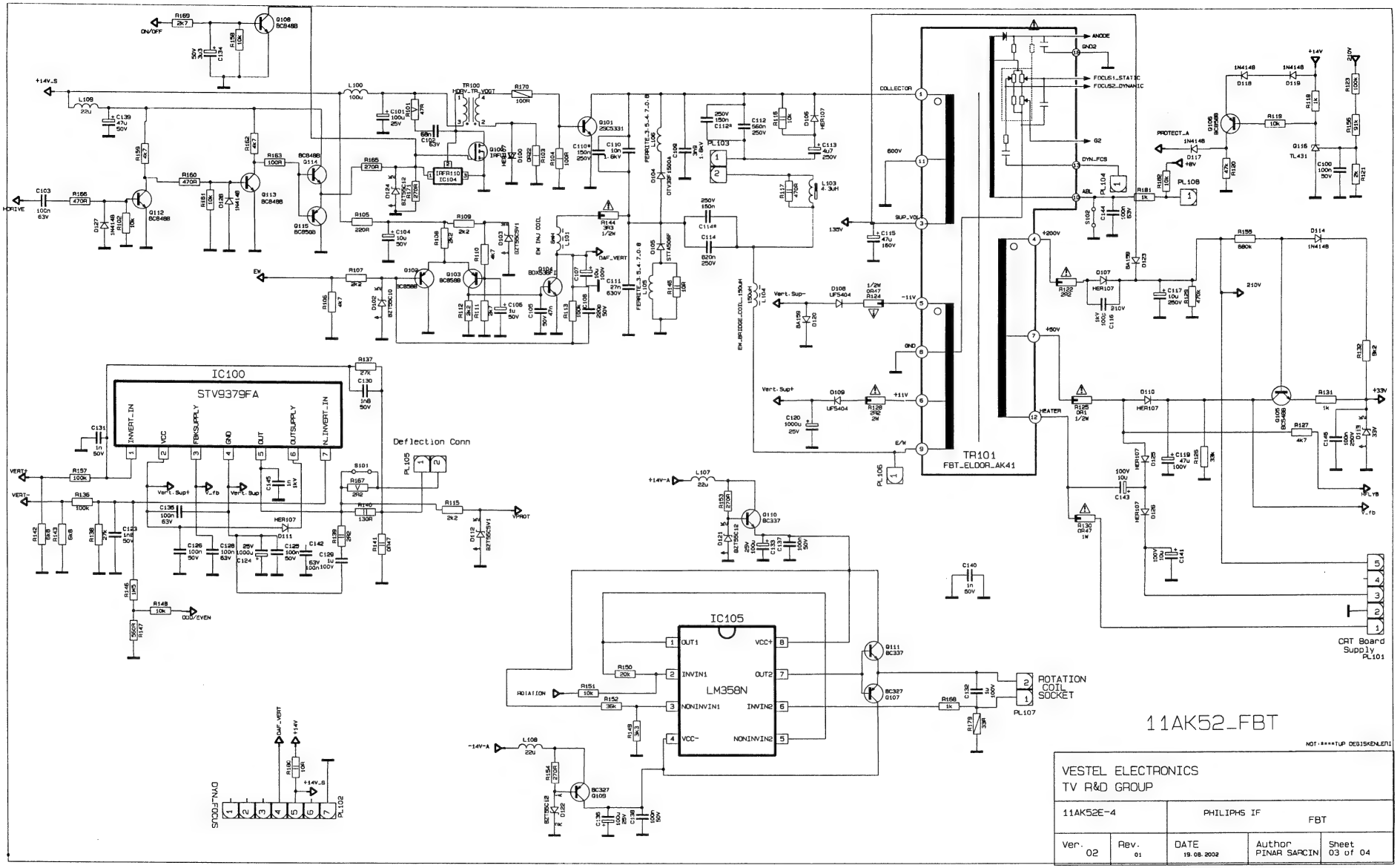

VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
100Hz-Audio Amplifier
Ver. 01
Rev.
DATE 19.08.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
MUTE
MAIN_OUT_L
MAIN_OUT_R
OPTIONAL
JACK_V2P
JK400
PL401
PL403
PL404
PL405
PL406
PL408
PL409
PL410
PL413
PL414
PL415
PL416
PL417
PL418
PL419
PL420
PL421
+5V
SCL
SDA
SERVICE
+14V-A
-14V-A
FERIT_6X20
FERIT_5X20
D404
1N4148
BC858B
0400
S401
S402
S408
S409
S410
S411
S412
S413
S414
S415
S416
S418
S419
S420
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV-LINK
IC_RESET
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
VPROT
+12V
DFVBL
HDRIVE
PROTECTION
VBSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS
SC3_CVBS_IN
SC3_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC2_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
OSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
OSS_PIP
MAIN_OUT_R
MAIN_OUT_L
SVHS_Y
SVHS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT

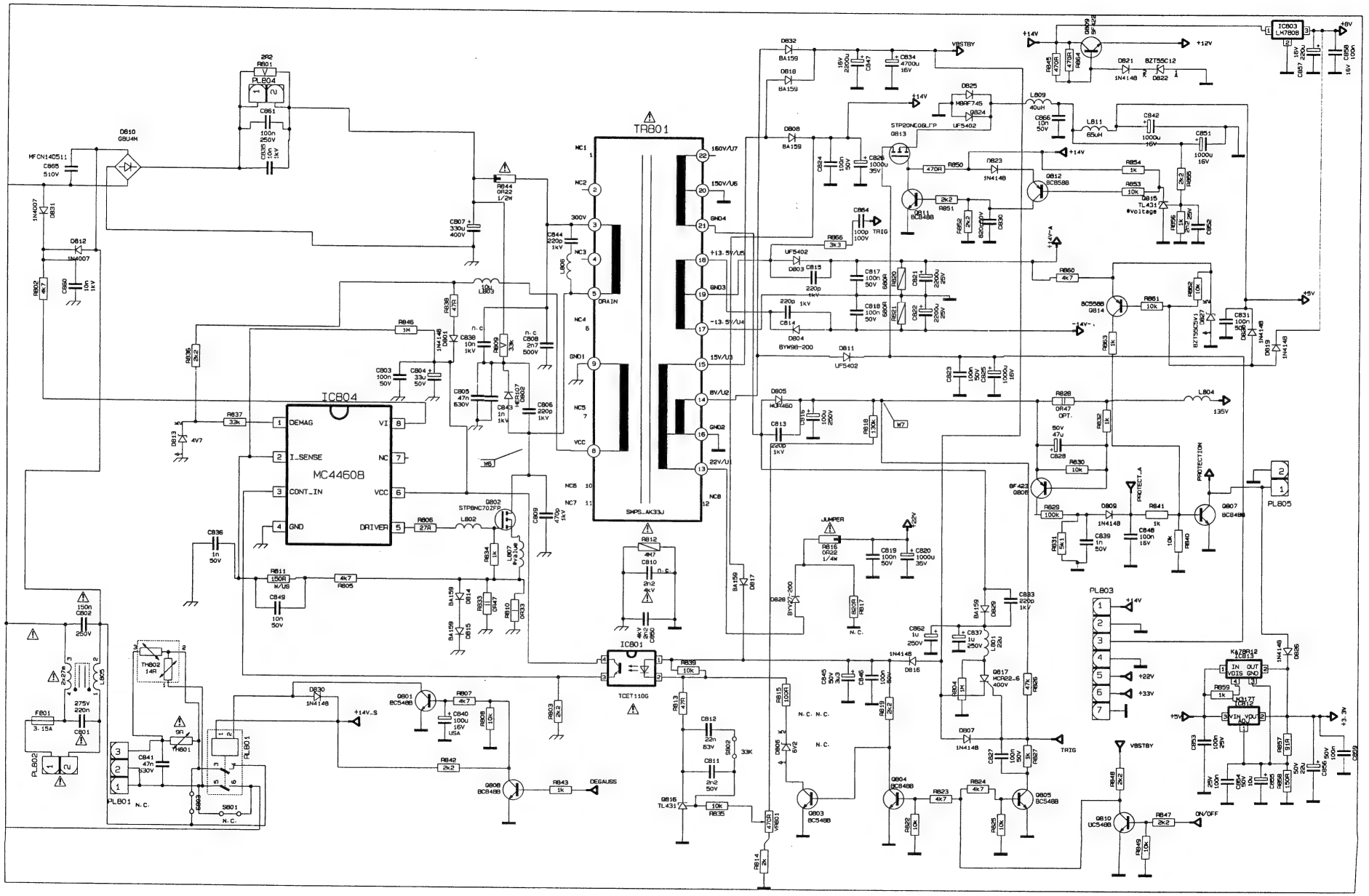

IC100
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
VCC+
INVIN1
OUT2
NONINVIN1
INVIN2
VCC-
NONINVIN2
ROTATION
ROTATION COIL SOCKET
PL107
TR101
FBT_ELDOR_AK41
ANODE
GND2
FOCUS1_STATIC
FOCUS2_DYNAMIC
G2
DYN_FCS
ABL
COLLECTOR
BUP_VOL
HEATER
E/W
CRT Board Supply
PL101
DYN_FOCUS
PL102
11AK52_FBT
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2
FBT
Ver. 02
Rev. 01
DATE 19.08.2002
Author PINAR SARCIN
Sheet 03 of 04

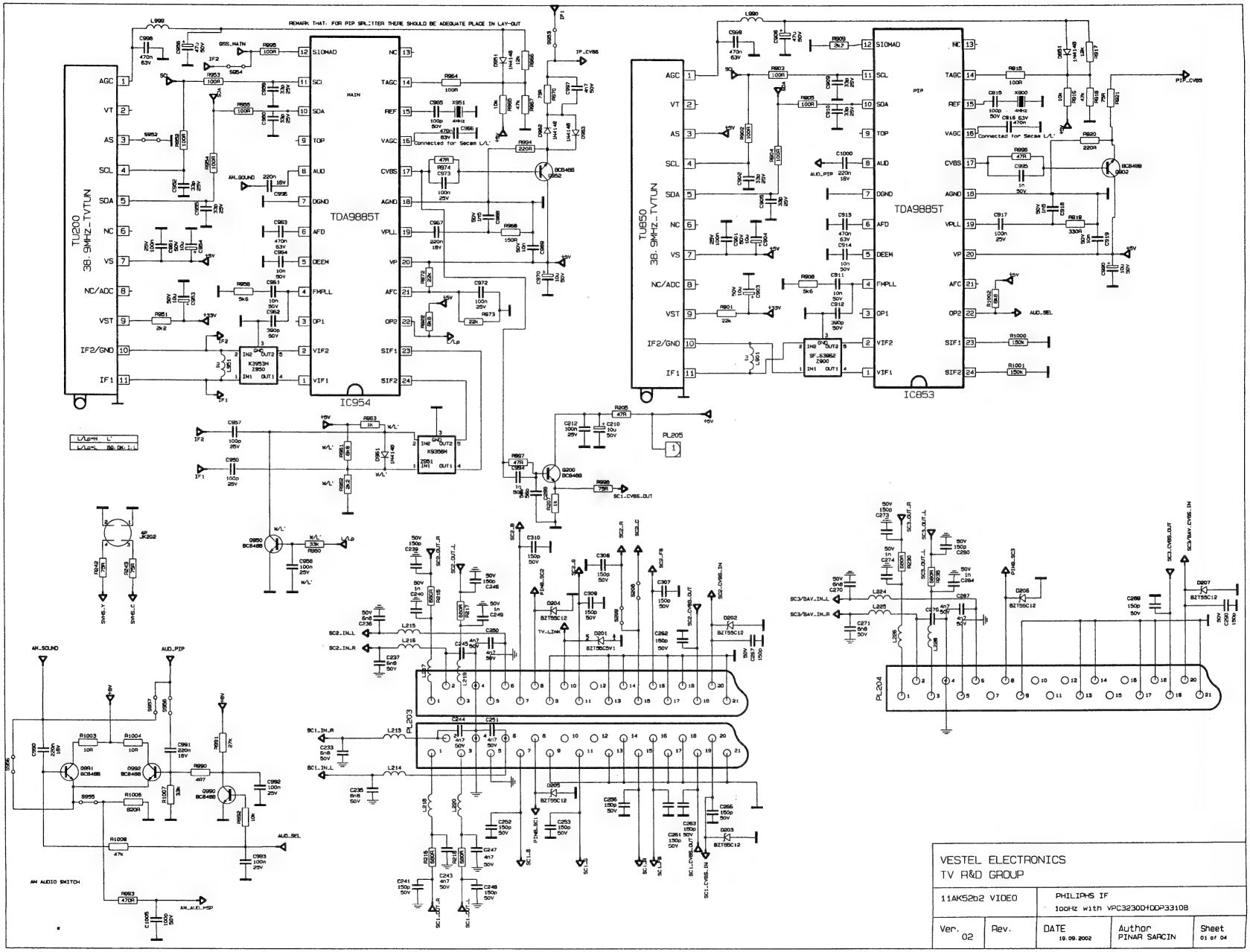

TR801
IC804
MC44608
IC801
TCET110G
SMPS_AK33J
STP8NC70ZFP
STP20NE06LFP
MBRF745
UF5402
BYW98-200
BC548B
BC558B
TL431
BZT55C12
1N4148
1N4007
6BU4M
MCR22-6
KA7812
KA7805
LM317
L7808
PL801
PL802
PL803
PL804
PL805
TH801
TH802
S801
IC803
IC813
+14V
+12V
+22V
+33V
+5V
+3.3V
+8V
135V
VBSTBY
TRIG
ON/OFF
DEGAUSS
PROTECTION
JUMPER

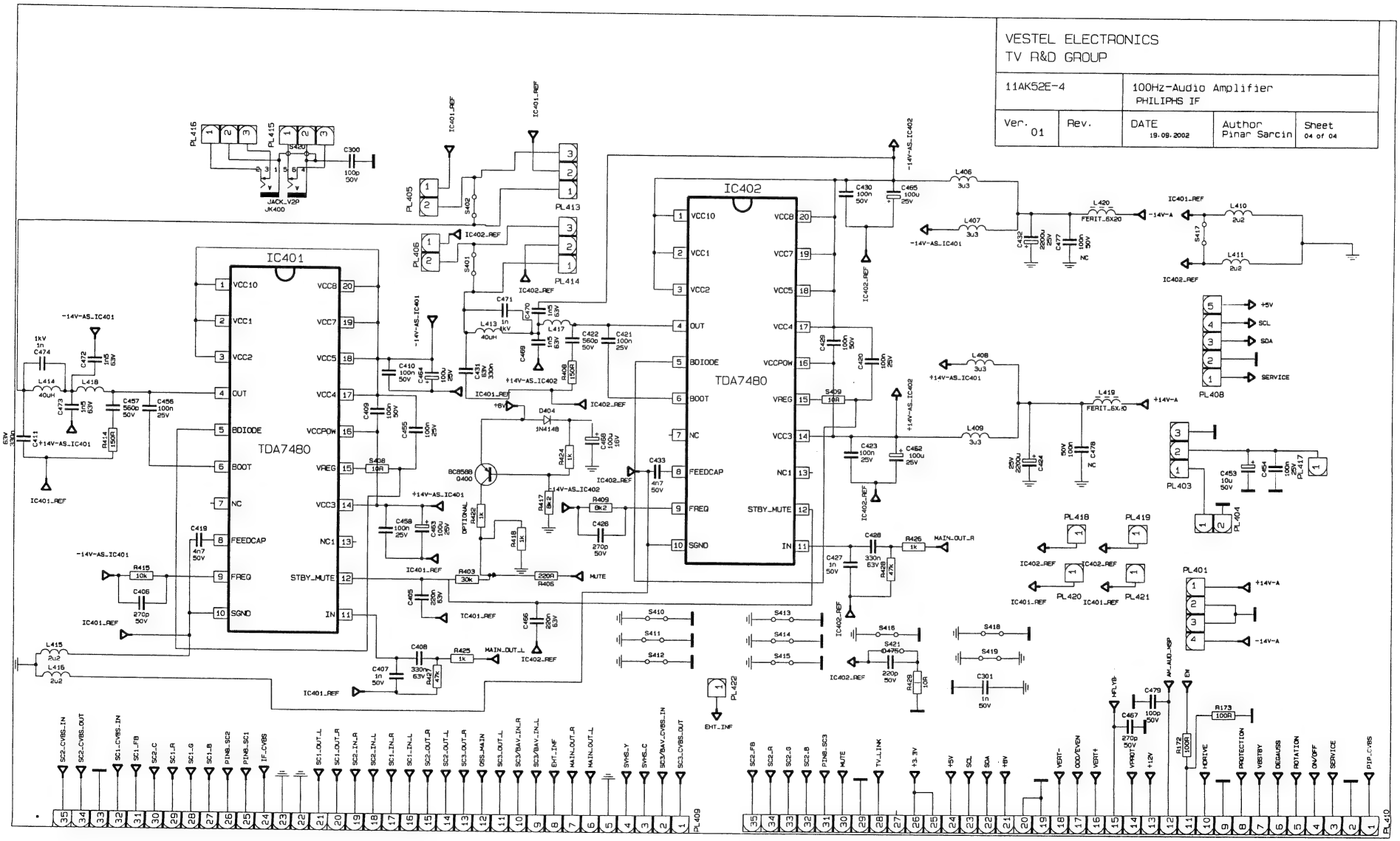

REMARK THAT: FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHz_TVTUN
TU201
38.9MHz_TVTUN
IC200
DRX3960A
IC201
DRX3960A
AGC
VT
AS
SCL
SDA
NC
VS
NC/ADC
VST
IF2/GND
IF1
TUNAGC
TUNAGC_PIP
IC_RESET
IF_CVBS
PIP_CVBS
SC1_CVBS_OUT
SC2_IN_L
SC2_IN_R
SC3/BAV_IN_L
SC3/BAV_IN_R
PL203
PL204
PL205
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-2 VIDEO
100Hz with VPC3230D+DDP3310B
Ver. 02
Rev.
DATE 19.08.2002
Author PINAR SARCIN
Sheet 01 of 04

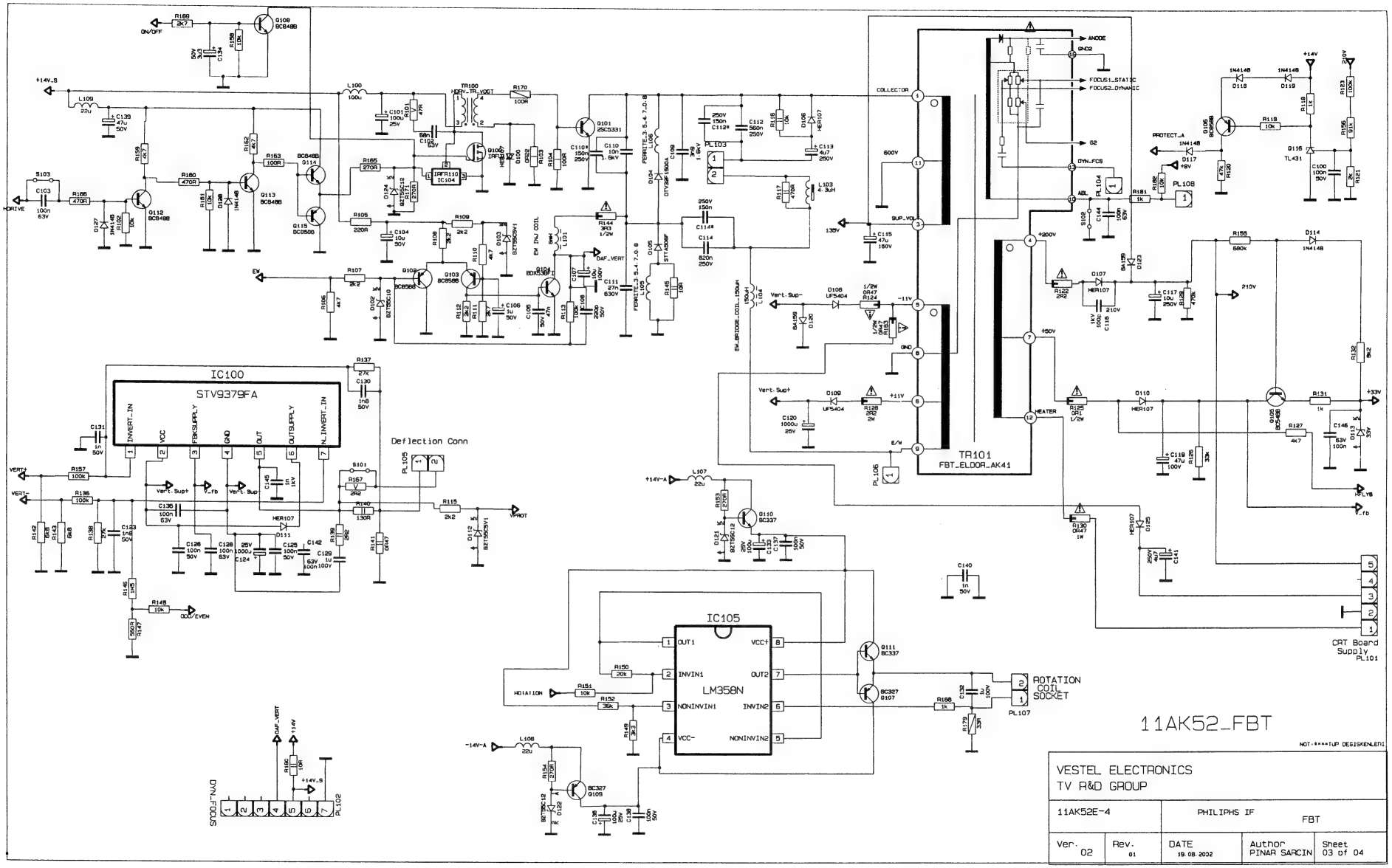

VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 01
Rev.
DATE 19.09.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
+8V
+5V
SCL
SDA
SERVICE
MUTE
MAIN_OUT_L
MAIN_OUT_R
EHT_INF
+14V-A
-14V-A
PL401
PL403
PL404
PL405
PL406
PL408
PL409
PL410
PL413
PL414
PL415
PL416
PL417
PL418
PL419
PL420
PL421
PL422
JK400
S401
S402
S420
D404
1N4148
BC858B
Q400
SC2_CVBS_IN
SC2_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC2_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
OSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
EHT_INF
MAIN_OUT_R
MAIN_OUT_L
SVHS_Y
SVHS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV_LINK
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
VFLYB
VFRQTC
+12V
MM_AUD_MSP
EW
HDRIVE
PROTECTION
VBSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS


IC100
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
XL_INVERT_IN
Deflection Conn
TR101
FBT_ELDOR_AK41
IC105
LM358N
ROTATION COIL SOCKET
CRT Board Supply PL101
11AK52_FBT
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
PHILIPHS IF
FBT
Ver. 02
Rev. 01
DATE 19.08.2002
Author PINAR SARCIN
Sheet 03 of 04


IC804
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
TR801
SMPS_AK33J
IC801
TCET110G
IC803
LM7808
PL803
PL804
PL805
PL801
PL802
STP20NE06LFP
STPBNC70ZFP
MC44608
TL431
BC548B
BC558B
BZT55C12
1N4148
UF5402
BA159
BYV27-200
MCR22-6
TRIG
DEGAUSS
ON/OFF
JUMPER
PROTECTION
PROTECT_A
+14V
+12V
+8V
+22V
+33V
+3.3V
VBSTBY
+14V_S
+14V_A
-14V_A
160V/U7
150V/U6
+13.5V/U5
-13.5V/U4
15V/U3
8V/U2
22V/U1
DRAIN
MFCN140511


REMARK THAT: FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHZ_TVTUN
TDA9885T
MAIN
IC954
TU850
38.9MHZ_TVTUN
TDA9885T
PIP
IC853
AM_SOUND
AUD_PIP
AUD_SEL
AM AUDIO SWITCH
PL203
PL204
PL205
SC1_CVBS_OUT
SC2_CVBS_OUT
SC3/BAV_IN_L
SC3/BAV_IN_R
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b2 VIDEO
PHILIPHS IF
100Hz with VPC3230D+DDP3310B
Ver. 02
Rev.
DATE 19.09.2002
Author PINAR SARCIN
Sheet 01 of 04


VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 01
Rev.
DATE 19.09.2002
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
VCC10
VCC1
VCC2
OUT
BDIODE
BOOT
NC
FEEDCAP
FREQ
SGND
VCC8
VCC7
VCC5
VCC4
VCCPOW
VREG
VCC3
NC1
STBY_MUTE
IN
-14V-AS_IC401
-14V-AS_IC402
+14V-AS_IC401
+14V-AS_IC402
IC401_REF
IC402_REF
MUTE
MAIN_OUT_L
MAIN_OUT_R
PL405
PL413
PL414
PL415
PL416
PL408
PL403
PL404
PL417
PL418
PL419
PL420
PL421
PL401
PL422
PL409
PL410
JACK_V2P
JK400
S420
S401
S402
S417
+5V
SCL
SDA
SERVICE
+14V-A
-14V-A
EHT_INF
SC2_CVBS_IN
SC2_CVBS_OUT
SC1_CVBS_IN
SC1_FB
SC2_C
SC1_R
SC1_G
SC1_B
PIN8_SC2
PIN8_SC1
IF_CVBS
SC1_OUT_L
SC1_OUT_R
SC2_IN_R
SC3_IN_L
SC1_IN_R
SC1_IN_L
SC2_OUT_R
SC2_OUT_L
SC3_OUT_R
OSS_MAIN
SC3_OUT_L
SC3/BAV_IN_R
SC3/BAV_IN_L
EHT_INF
MAIN_OUT_R
MAIN_OUT_L
SYNS_Y
SYNS_C
SC3/BAV_CVBS_IN
SC3_CVBS_OUT
SC2_FB
SC2_R
SC2_G
SC2_B
PIN8_SC3
MUTE
TV_LINK
+3.3V
+5V
SCL
SDA
+8V
VERT-
ODD/EVEN
VERT+
HFLYB
VPROT
+12V
AV_AUD_MSP
EN
R172
100R
R173
100R
FORIVE
PROTECTION
VSTBY
DEGAUSS
ROTATION
ON/OFF
SERVICE
PIP_CVBS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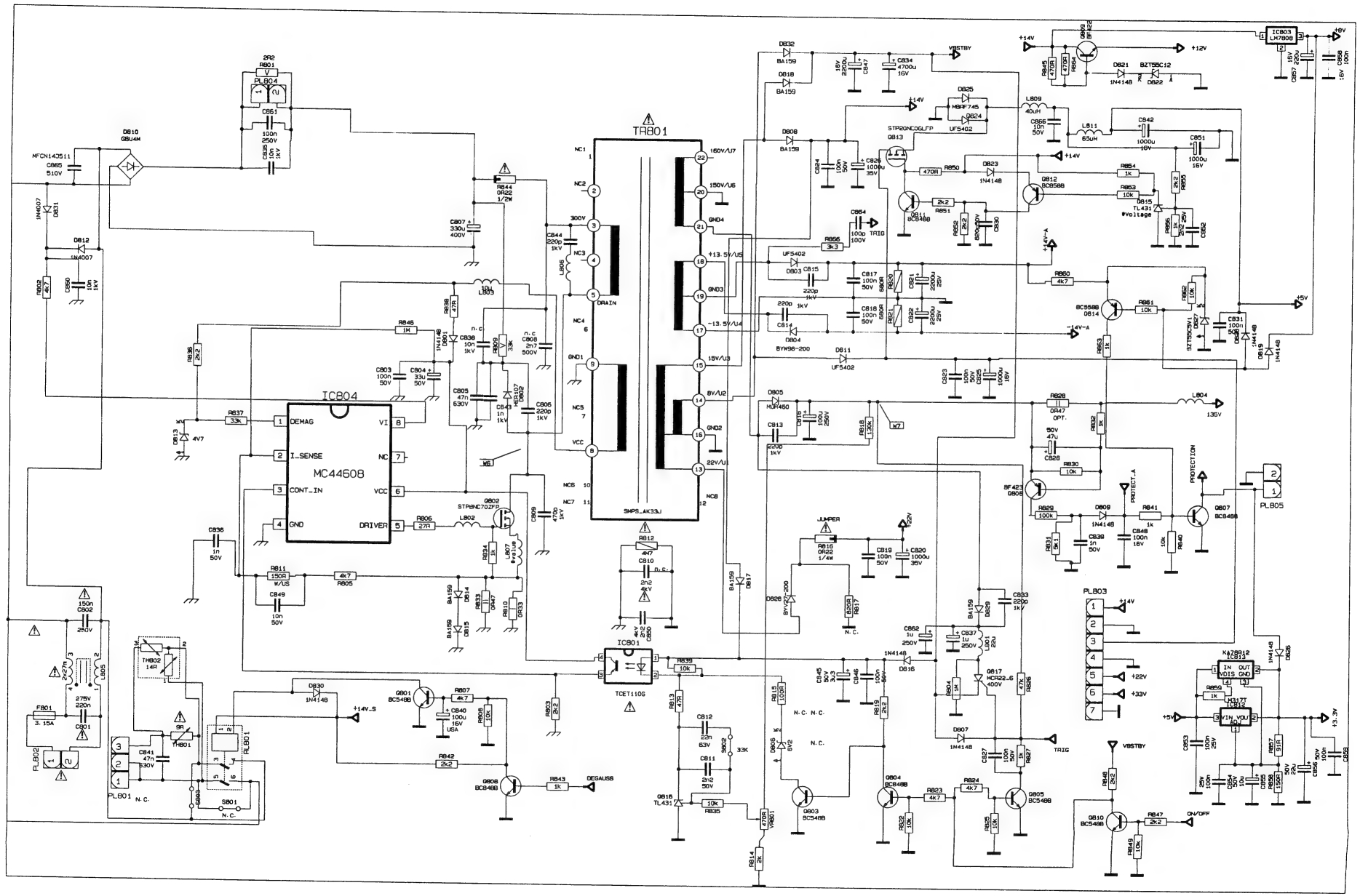
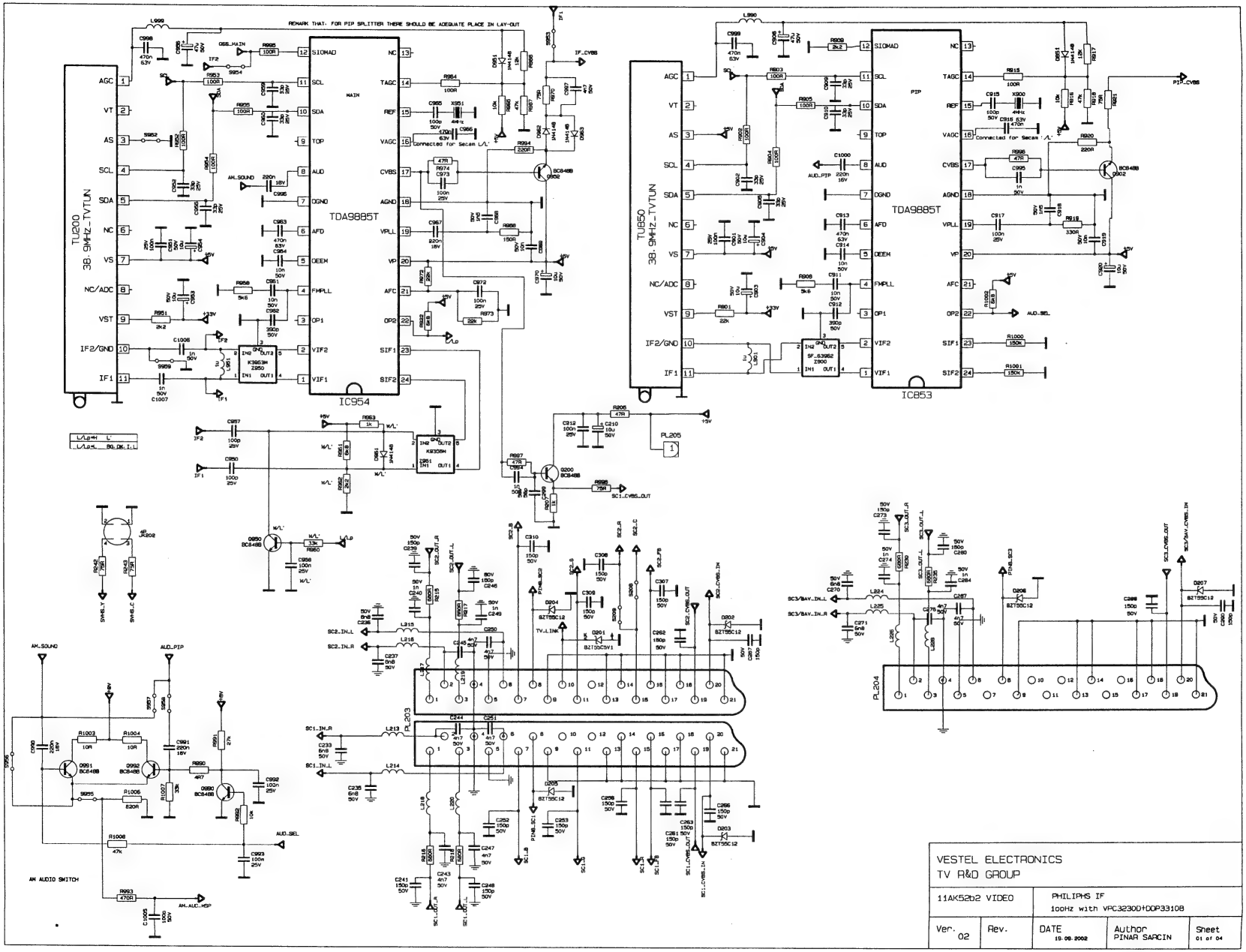
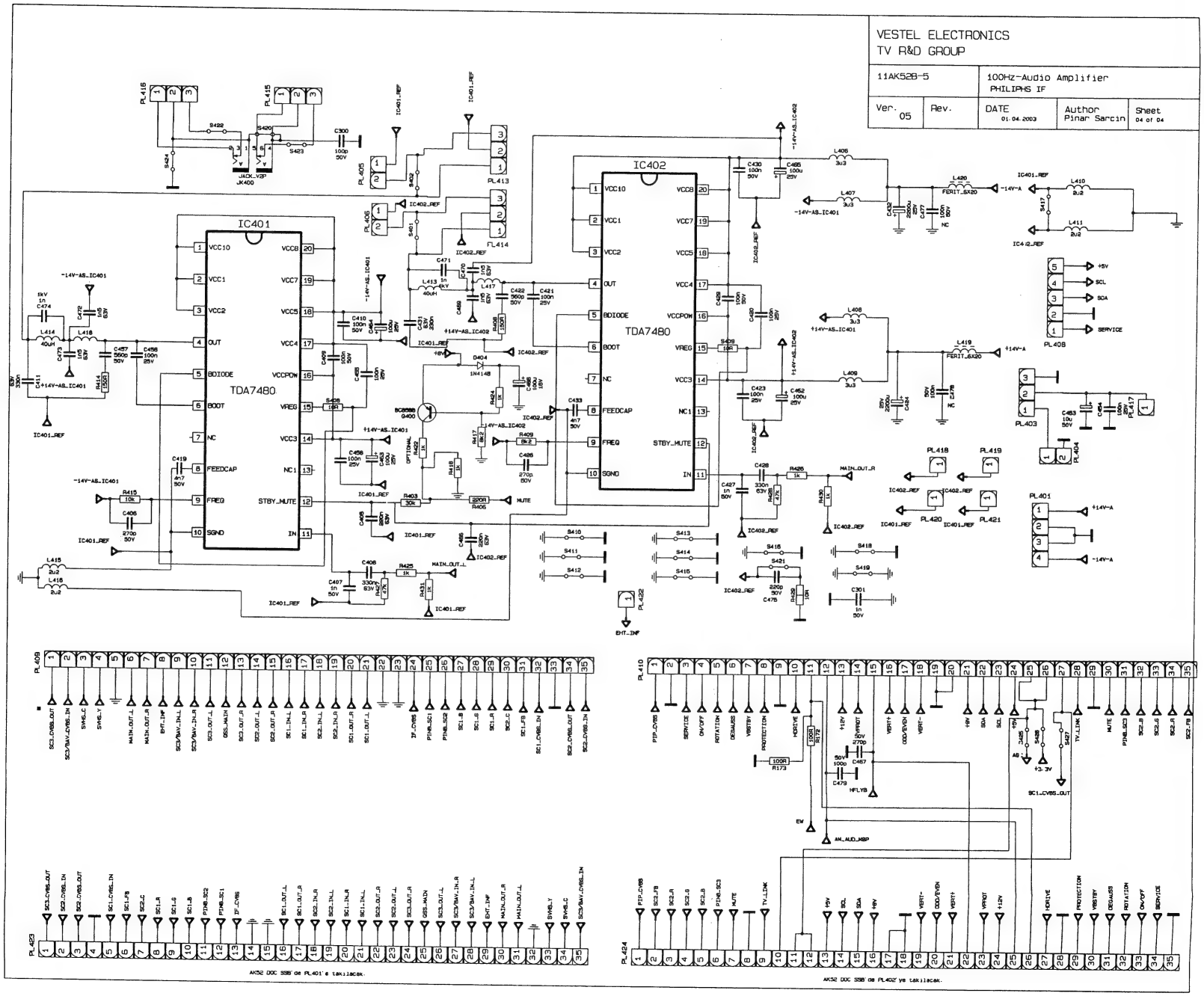
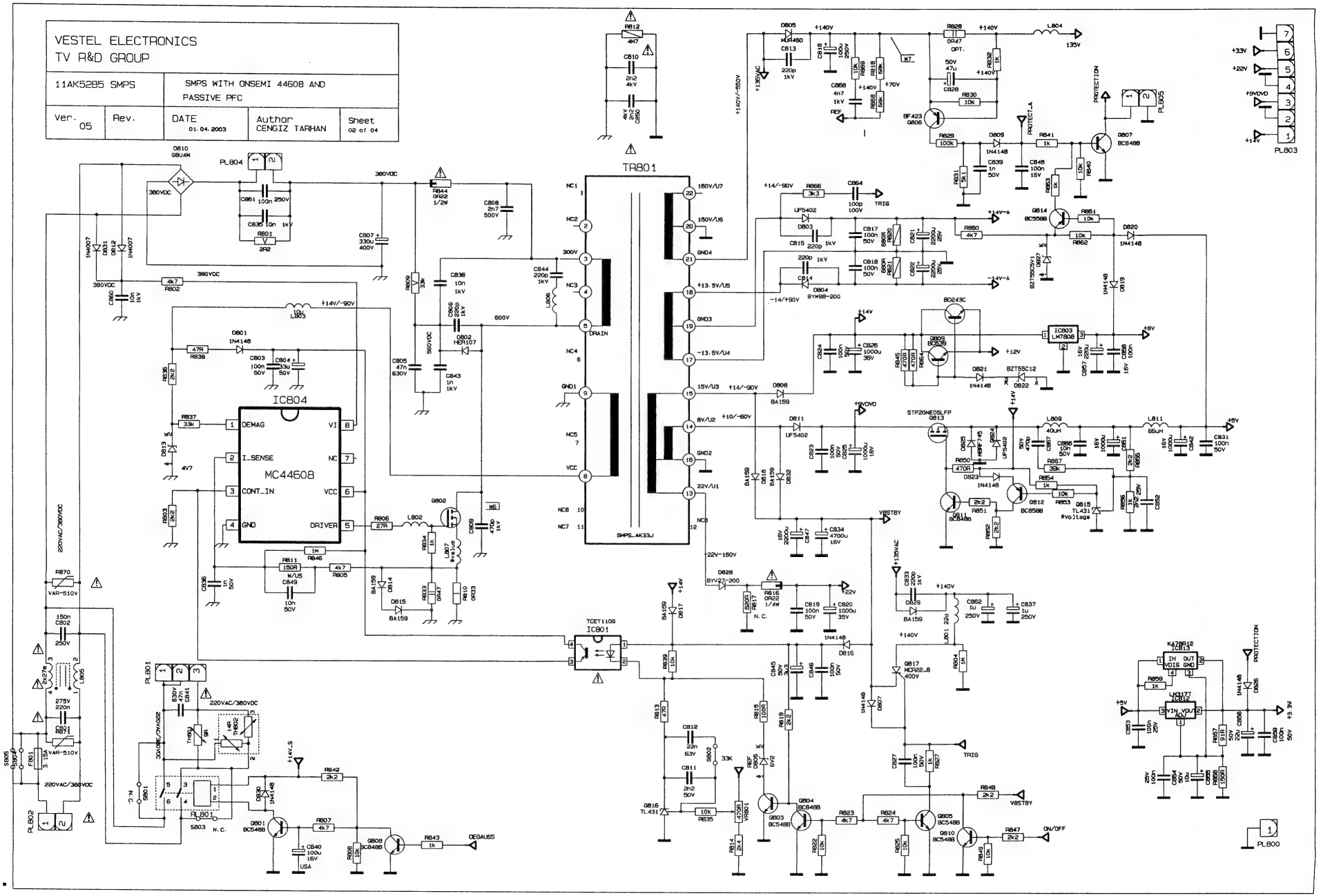
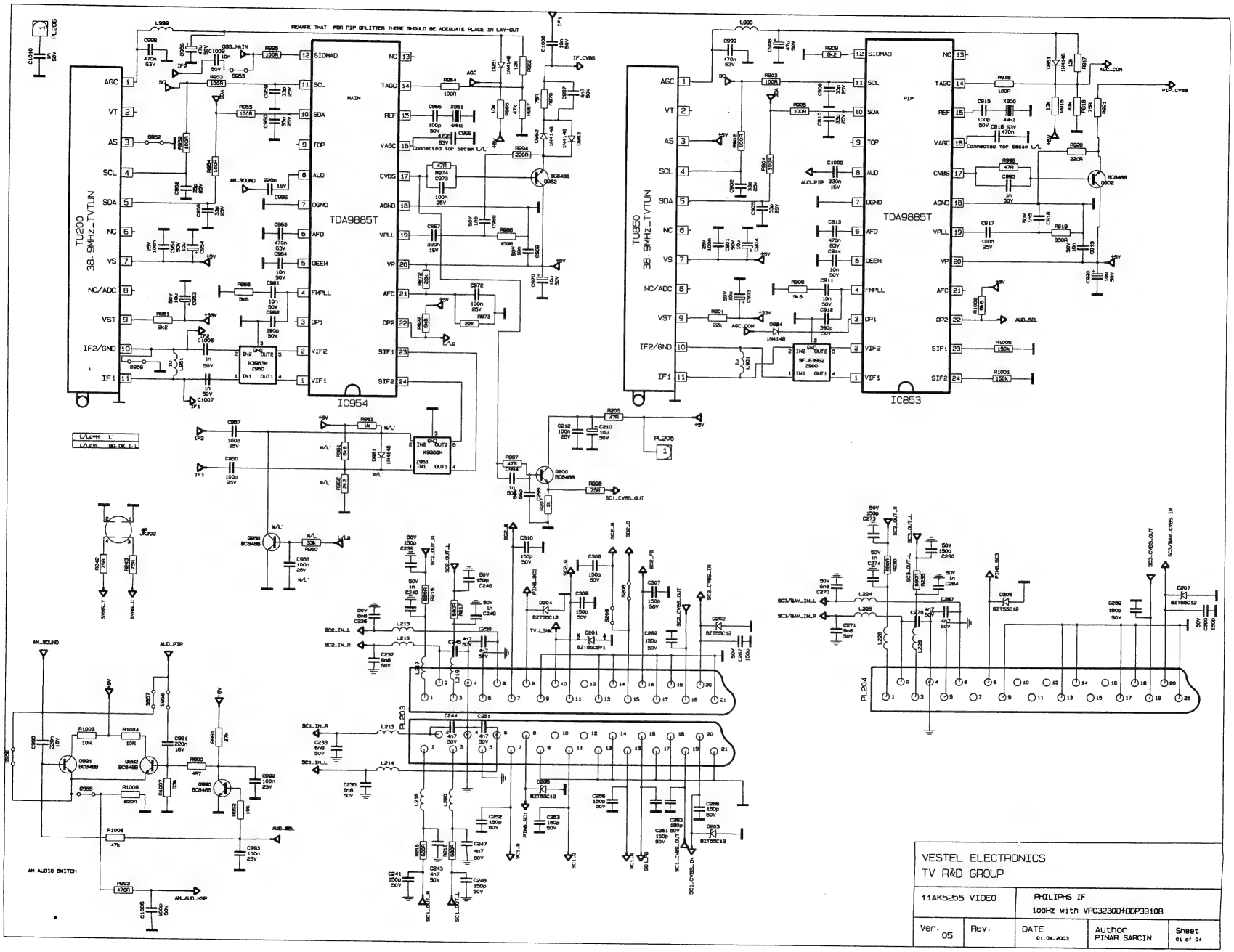
STV9379FA
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
NL_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
INVIN1
NONINVIN1
VCC-
VCC+
OUT2
INVIN2
NONINVIN2
ROTATION
TP101
FBT_ELDOR_AK41
ANODE
GND2
FOCUS1_STATIC
FOCUS2_DYNAMIC
G2
DYN_FCS
ABL
COLLECTOR
SUP_VCC
HEATER
CRT Board
Supply
PL101
ROTATION
COIL
SOCKET
PL107
11AK52_FBT
VESTEL ELECTRONICS
TV R&D GROUP
11AK52E-4
PHILIPHS IF
FBT
Ver.
02
Rev.
01
DATE
19.08.2002
Author
PINAR SARCIN
Sheet
03 of 04

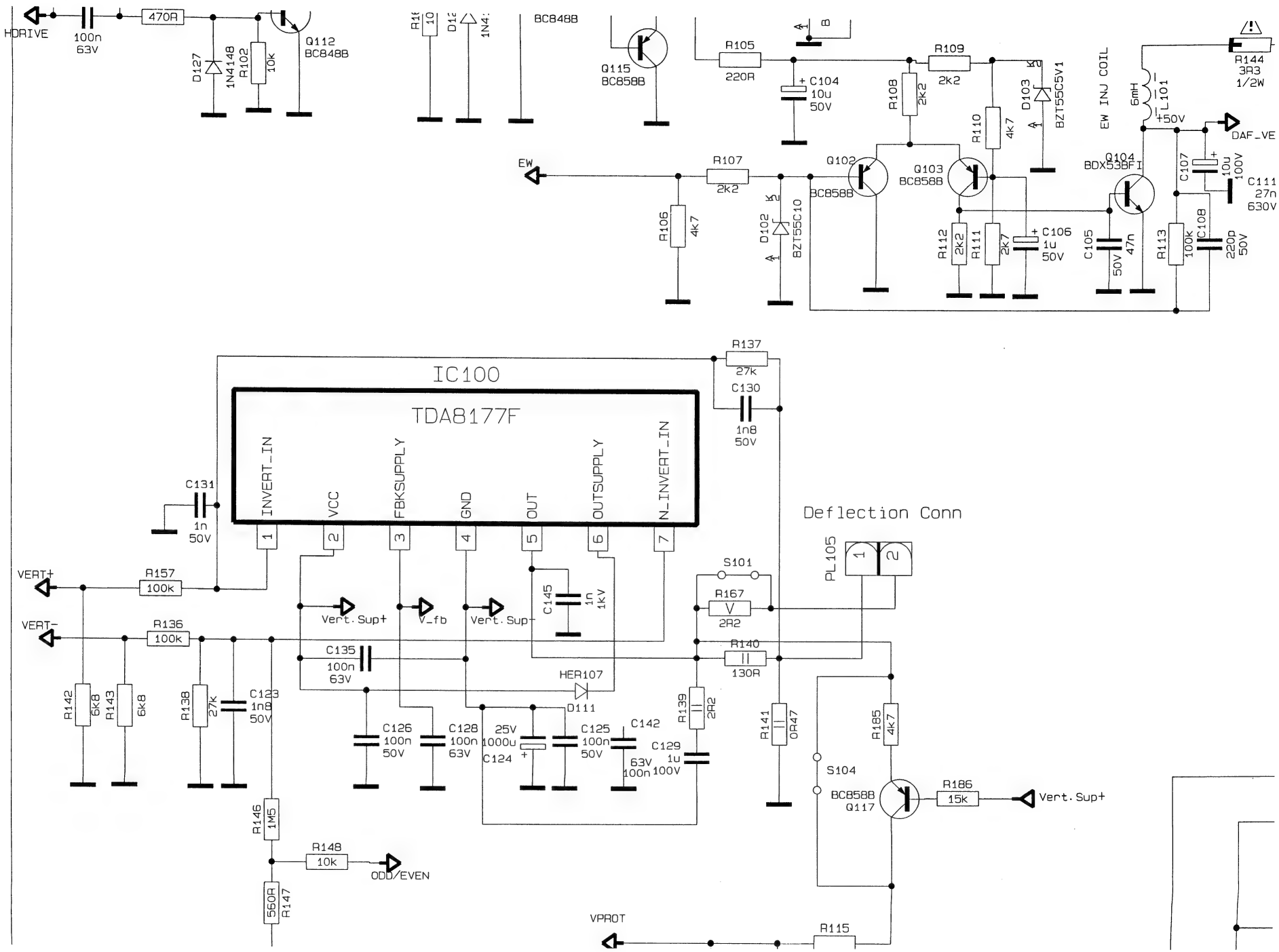

TA801
IC804
MC44608
IC801
TCET110G
IC803
LM7808
PL804
PL805
PL803
PL802
PL801
TH802
TH801
S801
DEMAG
I_SENSE
CONT_IN
GND
DRIVER
VI
NC
VCC
DRAIN
SMPS_AK33J
STP8NC70ZFP
STP20NC60GLFP
MBRF745
UF5402
BA159
BY98-200
HER107
HUR460
BYV27-200
MCR22_6
BC548B
TL431
KA78R12
KA317T
+14V
+12V
+6V
+5V
+3.3V
+22V
+33V
VBSTBY
TRIG
DEGAUSS
ON/OFF
PROTECTION
PROTECT_A
JUMPER
N.C.
W/US
W6
W7

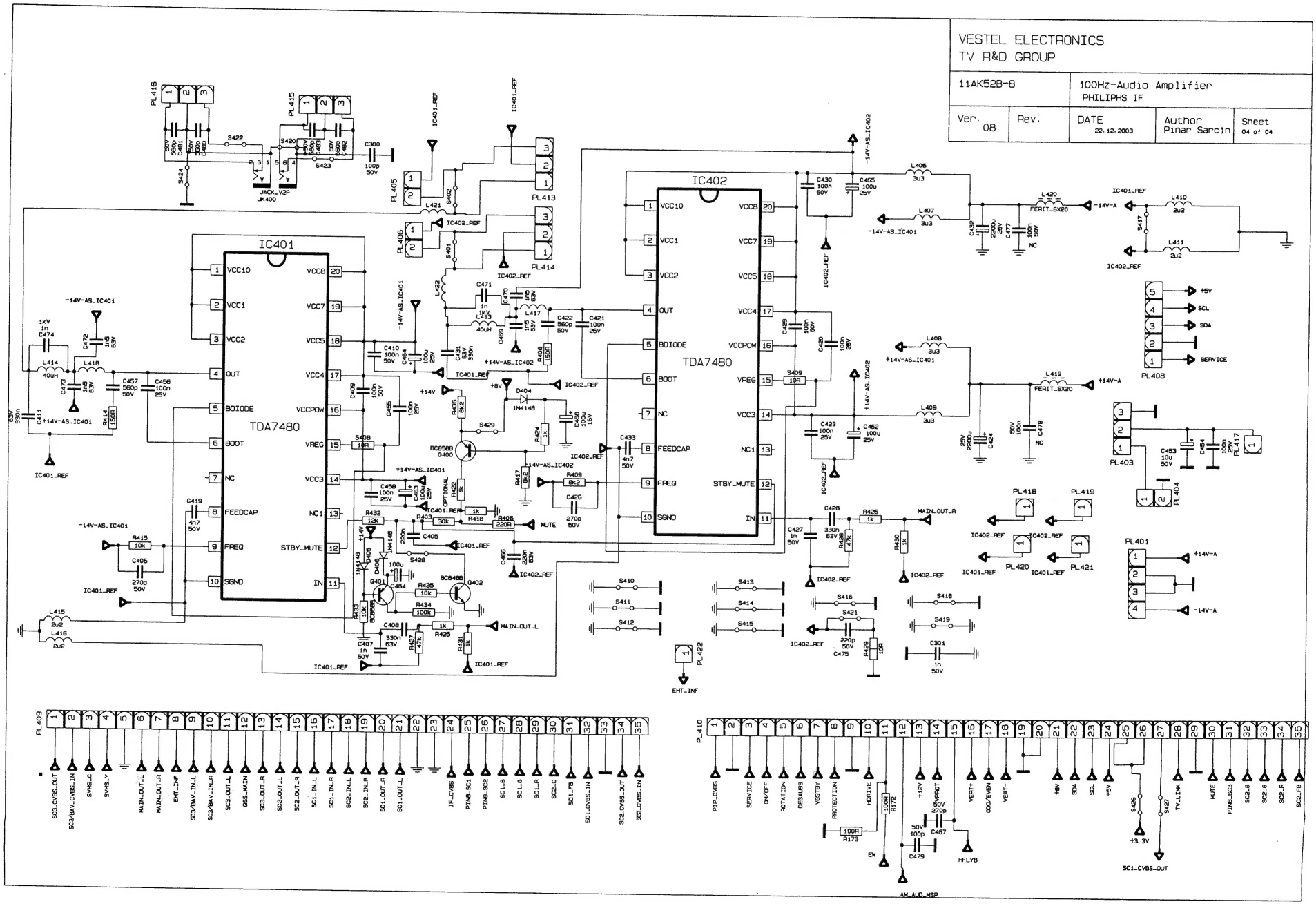

REMARK THAT: FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHZ_TVTUN
TDA9885T
MAIN
IC954
TU850
38.9MHZ_TVTUN
TDA9885T
PIP
IC853
AM AUDIO SWITCH
PL203
PL204
PL205
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b2 VIDEO
PHILIPHS IF
100Hz with VPC3230D+DOP33108
Ver. 02
Rev.
DATE 19.06.2002
Author PINAR SARCIN
Sheet 01 of 04

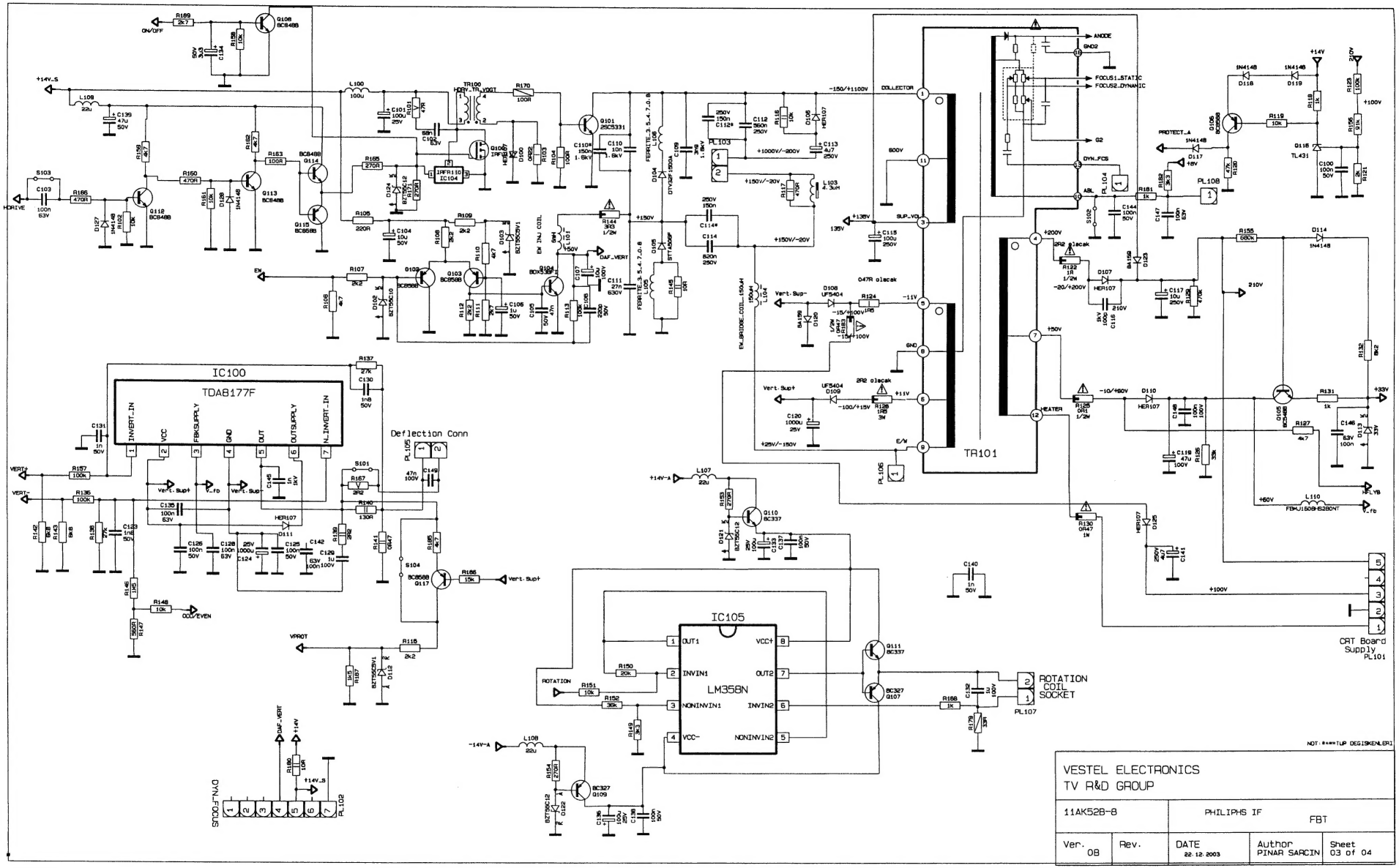

VESTEL ELECTRONICS
TV R&D GROUP
11AK52B-5
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 05
Rev.
DATE 01.04.2003
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
AK52 DOC SSB de PL401'e takılacak.
AK52 DOC SSB de PL402'ye takılacak.

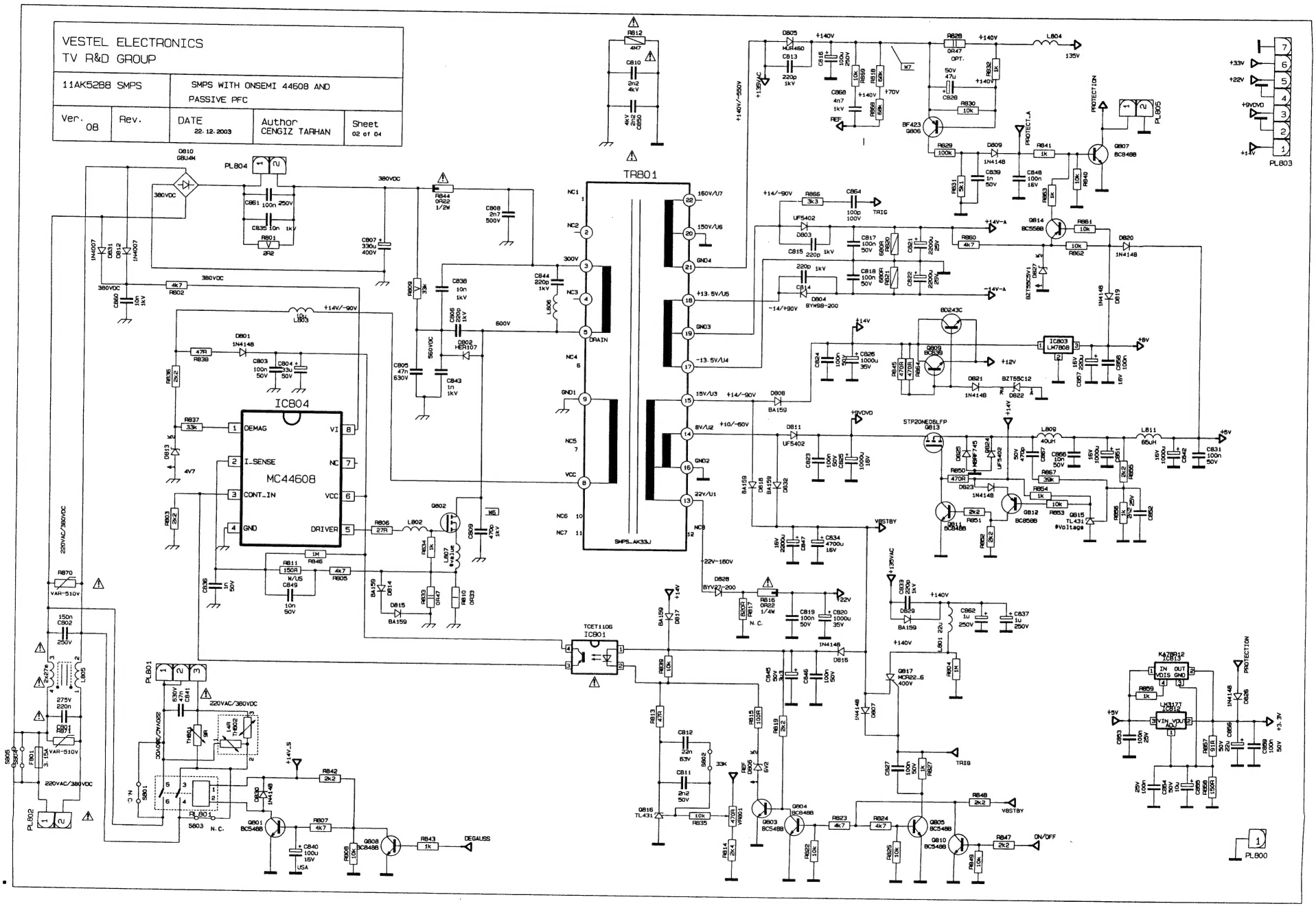

VESTEL ELECTRONICS
TV R&D GROUP
11AK5285 SMPS
SMPS WITH ONSEMI 44608 AND PASSIVE PFC
Ver. 05
Rev.
DATE 01.04.2003
Author CENGIZ TARHAN
Sheet 02 of 04
IC804
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
TR801
SMPS_AK33J
DRAIN
IC801
TCET1106
PL801
PL802
PL803
PL804
PL805
PL800
S801
S802
S803
S804
S805
DEGAUSS
ON/OFF
PROTECTION
PROTECT-A
TRIG
VBSTBY
135V
+140V
+14V
+8V
+12V
+5V
+3.3V
+33V
+22V
+9VDVD
380VDC
220VAC/380VDC
STP20NE60LFP
BC243C
BC548B
BC856B
BC848B
BF423
MCR22-8
TL431
LM7808
LM317
KA78R12
1N4148
BA159
BYV27-200
HER107
BYW98-200
UF5402
MUR460

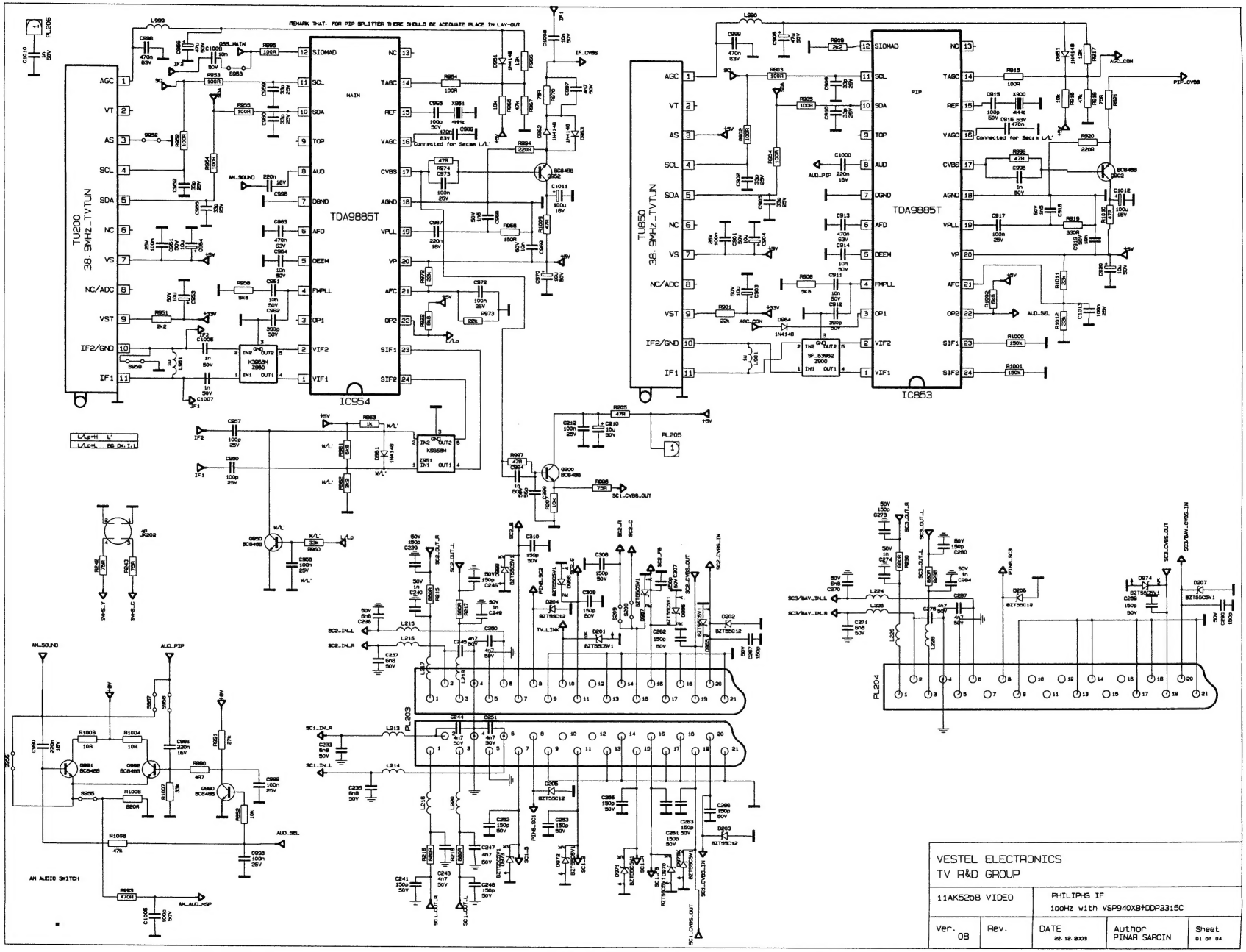

REMARK THAT: FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHZ_TVTUN
TDA9885T
MAIN
IC954
TU850
38.9MHZ_TVTUN
TDA9885T
PIP
IC853
AM AUDIO SWITCH
PL203
PL204
PL205
PL206
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b5 VIDEO
PHILIPHS IF
100Hz with VPC3230D+DDP3310B
Ver. 05
Rev.
DATE 01.04.2003
Author PINAR SARCIN
Sheet 01 of 04


HDRIVE
100n
63V
470R
D127
1N4148
R102
10k
Q112
BC848B
BC848B
Q115
BC858B
R105
220R
C104
10u
50V
R109
2k2
R108
2k2
D103
BZT55C5V1
R110
4k7
EW INJ COIL
6mH
L101
R144
3R3
1/2W
+50V
DAF_VE
EW
R107
2k2
R106
4k7
D102
BZT55C10
Q102
BC858B
Q103
BC858B
Q104
BDX53BFI
R112
2k2
R111
2k7
C106
1u
50V
C105
50V
47n
R113
100k
C108
220p
50V
C107
10u
100V
C111
27n
630V
IC100
TDA8177F
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
1
2
3
4
5
6
7
R137
27k
C130
1n8
50V
C131
1n
50V
Deflection Conn
PL105
S101
R167
2R2
R140
130R
VERT+
R157
100k
VERT-
R136
100k
Vert. Sup+
V_fb
Vert. Sup-
C145
1n
1kV
C135
100n
63V
HER107
D111
R142
6k8
R143
6k8
R138
27k
C123
1n8
50V
C126
100n
50V
C128
100n
63V
25V
1000u
C124
C125
100n
50V
C142
63V
100n
C129
1u
100V
R139
2R2
R141
0R47
R185
4k7
S104
BC858B
Q117
R186
15k
Vert. Sup+
R146
1M5
R148
10k
ODD/EVEN
560R
R147
VPROT
R115


VESTEL ELECTRONICS
TV R&D GROUP
11AK52B-8
100Hz-Audio Amplifier
PHILIPHS IF
Ver. 08
Rev.
DATE 22.12.2003
Author Pinar Sarcin
Sheet 04 of 04
IC401
IC402
TDA7480
PL401
PL402
PL403
PL404
PL405
PL406
PL407
PL408
PL409
PL410
PL413
PL414
PL415
PL416
PL418
PL419
PL420
PL421
PL422
JACK_V2P
JK400
EHT_INF
AM_AUD_MSP
SC1_CVBS_OUT
SC2_CVBS_OUT
SC3_CVBS_OUT
SC3/BAV_CVBS_IN
SVHS_C
SVHS_Y
MAIN_OUT_L
MAIN_OUT_R
SC3/BAV_IN_L
SC3/BAV_IN_R
SC3_OUT_L
OSS_MATV
SC3_OUT_R
SC2_OUT_L
SC2_OUT_R
SC1_IN_L
SC1_IN_R
SC2_IN_L
SC2_IN_R
SC1_OUT_R
SC1_OUT_L
IF_CVBS
PINS_SC1
PINS_SC2
SC1_B
SC1_G
SC1_R
SC2_C
SC1_FB
SC1_CVBS_IN
SC2_CVBS_IN
PIP_CVBS
SERVICE
ON/OFF
ROTATION
DEGAUSS
VBSTBY
PROTECTION
HDRIVE
+12V
VPROT
VERT+
ODD/EVEN
VERT-
+8V
SDA
SCL
+5V
TV_LINK
MUTE
PINS_SC3
SC2_B
SC2_G
SC2_R
SC2_FB
+5V
SCL
SDA
SERVICE
+14V-A
-14V-A
MUTE
MAIN_OUT_R
MAIN_OUT_L
+3.3V
EW
HFLYB


IC100
TDA8177F
INVERT_IN
VCC
FBK/SUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
Deflection Conn
IC105
LM358N
OUT1
INVIN1
NONINVIN1
VCC-
VCC+
OUT2
INVIN2
NONINVIN2
TR101
COLLECTOR
SUP_VO
GND
HEATER
E/W
ANODE
G2
ABL
ROTATION COIL SOCKET
CRT Board Supply PL101
VESTEL ELECTRONICS
TV R&D GROUP
11AK52B-8
PHILIPHS IF
FBT
Ver. 08
Rev.
DATE 22.12.2003
Author PINAR SARCIN
Sheet 03 of 04


VESTEL ELECTRONICS
TV R&D GROUP
11AK5288 SMPS
SMPS WITH ONSEMI 44608 AND PASSIVE PFC
Ver. 08
Rev.
DATE 22.12.2003
Author CENGIZ TARHAN
Sheet 02 of 04
IC804
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
TRB01
SMPS_AK33J
DRAIN
IC801
TCET1106
PL804
PL803
PL805
PL802
PL801
PL800
PROTECTION
PROTECT_A
STP20NE08LFP
IC803 LM7808
IC802 KA78R12
IC813 LM317
TRIG
DEGAUSS
ON/OFF
VBSTBY
220VAC/380VDC
380VDC
135V
+140V
+14V
+12V
+8V
+5V
+3.3V
+33V
+22V
+9VDVD
-14V-A
+14V-A


REMARK THAT. FOR PIP SPLITTER THERE SHOULD BE ADEQUATE PLACE IN LAY-OUT
TU200
38.9MHz_TVTUN
TDA9885T
MAIN
IC954
TU850
38.9MHz_TVTUN
TDA9885T
PIP
IC853
AGC
VT
AS
SCL
SDA
NC
VS
NC/ADC
VST
IF2/GND
IF1
SIOMAD
SCL
SDA
TOP
AUD
DGND
AFD
DEEM
FMPLL
OP1
VIF2
VIF1
NC
TAGC
REF
VAGC
CVBS
AGND
VPLL
VP
AFC
OP2
SIF1
SIF2
AM_SOUND
AUD_PIP
AUD_SEL
AM AUDIO SWITCH
AM_AUD_HSP
SC1_CVBS_OUT
SC1_CVBS_IN
SC2_CVBS_IN
SC3_CVBS_OUT
SC3/SAV_CVBS_IN
PL206
PL205
PL204
PL203
VESTEL ELECTRONICS
TV R&D GROUP
11AK52b8 VIDEO
PHILIPHS IF
100Hz with VSP940XB+DDP3315C
Ver. 08
Rev.
DATE 22.12.2003
Author PINAR SARCIN
Sheet 01 of 04